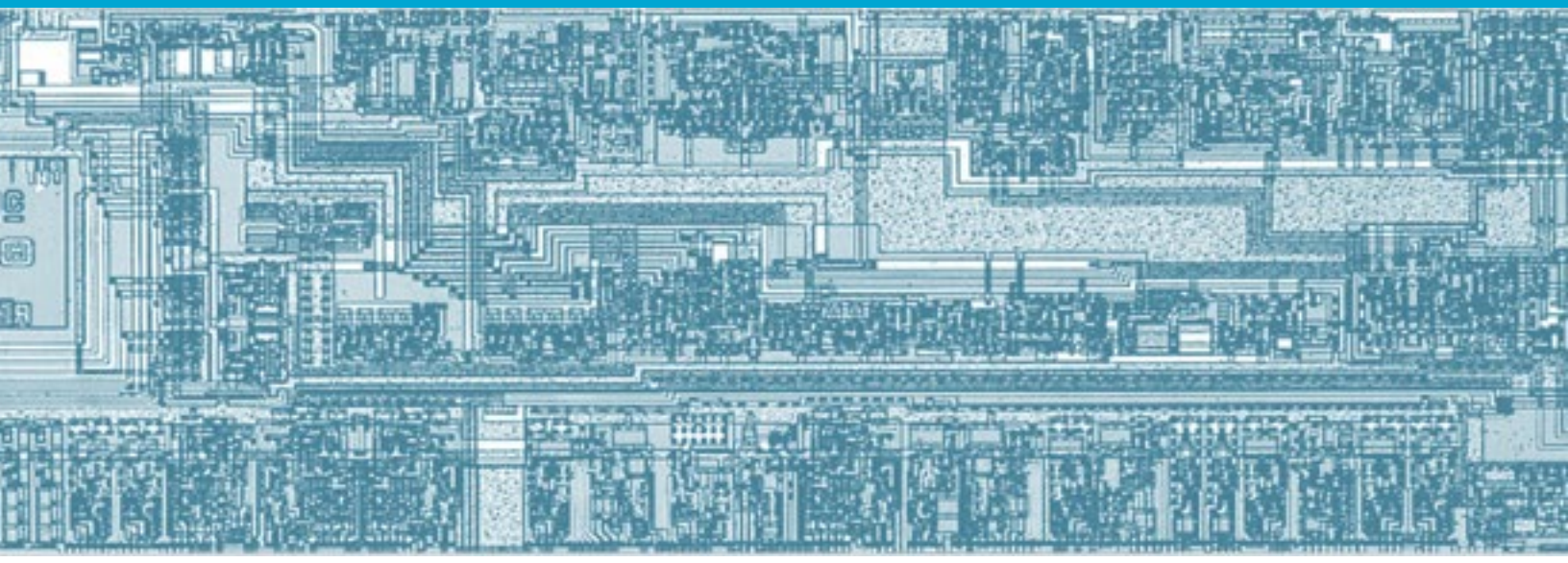
VOLUME 14 - WINTER 2022

SILICON STARTUP SOLUTIONS

it's about what's next.®

A SILICON CATALYST NEWSLETTER

A VALUABLE RESOURCE FOR THE SEMICONDUCTOR STARTUP COMMUNITY



VOLUME 14

IN THIS ISSUE

Silicon Catalyst Advisor Dave Dwelley, Former CTO of Maxim Integrated
page 26

From Strength to Strength

Lance Bell - Partner / Publisher

As a partner in Silicon Catalyst for the past 8 years, it is with much satisfaction that I announce that we have accepted our 90th Portfolio Company globally. It is humbling to think our former CEO Dan Armbrust is one of 24 members appointed to the Industrial Advisory Committee (IAC), an advisory body that will provide guidance to the US Secretary of Commerce on a range of issues related to domestic semiconductor research and development in support of CHIPS for America. In addition, our current CEO Pete Rodriguez served on the semiconductor working group of the President's Council of Advisors in Science and Technology (PCAST).

I am pleased to announce that top-tier venture capital firm Mayfield has become a Strategic Investment Partner and is joining forces with Silicon Catalyst to foster startup innovation. This follows the firm's 50+ year track record of investing in iconic semiconductor companies. By way of background, Mayfield has invested in more than 550 companies, resulting in 120 IPOs, more than 225 acquisitions, and currently has $2.2B under management. The collaboration follows Mayfield's conviction in the renaissance of silicon. Under the terms of the alliance with Silicon Catalyst, Mayfield will invest capital in and provide mentoring to the majority of seed stage companies admitted to the Silicon Catalyst Incubator/ Accelerator and will evaluate them for follow-on investments. Most seed stage companies will be eligible to receive $150K at admission into the Silicon Catalyst program.

In addition, we have formed a partnership with Luminate to speed development of emerging technologies. Luminate is the world's largest accelerator for startups developing optics, photonics, and imaging (OPI) enabled technologies. This partnership will help to close the development and manufacturing gaps that often exist when working across multiple technical disciplines to bring novel technologies to market. The partnership will also improve access to funding opportunities for early-stage companies. Qualifying startups developing OPI-based products receive $100,000 upon admission and have the chance to compete for up to $2 million on follow-on funding to support their growth.

We continue to drive thought leadership in our community through the Semiconductor Industry Forum, now in its fifth year, and our collaboration with the Ojo-Yoshida report. Interestingly, they featured our Portfolio Company OWL in a recent webinar. That same OWL is presenting their technology at US Ambassador to Japan Rahm Emanuel's place, yes, the same Rahm Emanuel that was Chief of Staff to former President Obama. How cool is that. Our goal is to take our companies from PowerPoint to powerhouse.

And last but certainly not least, we announced the appointment of Dr. Atiye Bayman as Partner. In particular, Dr. Bayman will be directly involved in the screening, selection and incubation of the entrepreneurial teams developing the next generation of MEMS devices and materials for semiconductors including those for life science applications.

WELCOME

CHAIRMAN'S CORNER
RICK LAZANSKY

Chairman and Co-Founder, Silicon Catalyst
Serial Entrepreneur and Incubator Fanatic

Looking back on eight years

Silicon Catalyst celebrated its 8th anniversary this year. Well, we didn't actually celebrate. I mean we were planning on having a 5th year party back in '20, but, you know, that pandemic and all got in the way. You might notice that the calendar math doesn't quite work – yes, the 5th birthday was planned for the 6th year.

We started Silicon Catalyst as an experiment, an outgrowth of our thinking that there should be more opportunities for our kind of hardware, but almost every last drop of venture capital was headed to software startups. Retrospectively, back in the 80's it was a surprisingly level playing field. Let's call it $10M to start either a well-financed then-called-Series-A software startup or a hardware startup. By the 2010s software was 2 orders of magnitude lower, and IC startups were on their way to 2 orders more.

We wanted to try to change that. We did the lean canvas thing – and talked to a lot of people, ran some surveys, made some adjustments, and dove in. We agreed when folks said we were crazy. That's exactly the headwind some want when launching a startup. Because competition is not in sight, and they winds are bound to change.

Looking at the historical semi-conductor-related VC investments data included from the PCAST report issued by the White House in September can give you a sense of the challenges faced by semiconductor startups in their hunt for initial funding beyond their traditional family-and friends outreach for seed-stage funding. Interesting to note that within the $11B appropriation for semiconductor R&D in the CHIPS Act is Recommendation #6:

"The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups."

"The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500 million to provide financial support and in-kind access to prototyping and tools for semiconductor startups."

We're all hopeful that 2022 will be the low-water mark and the 2030 graph of VC investments in the semiconductor industry will look more like a bathtub curve.

Whether there's a party or not in the future, there is cause for celebration. Silicon Catalyst has engaged with close to 1000 early-stage entrepreneurial teams, resulting in 400+ applications, with a 10% admissions rate; more than 250 advisors from the industry to help us select and coach them; a dozen strategic corporate partners; 60 in-kind partners; strong relationships with several dozen universities (where a third of our startups originate). The winds have changed.

There is a lot to say about the adjustments we've made. An example is whether we were looking for IC startups that would design and sell chips, IP companies that would develop and offer IP, or solutions companies, that would make ICs because they needed them at the core of a solution that they would market. We've learned that there's not one answer – all 3 are valid, and part of our job became helping our startups learn what was right for them. The team has its biases. Those startups that favor "chips for sale" quickly learn that there is still a lot of software and platform needed, a truth learned by IBM, then again by Intel. Those that choose IP learn that demonstrating working hardware is required. I favor

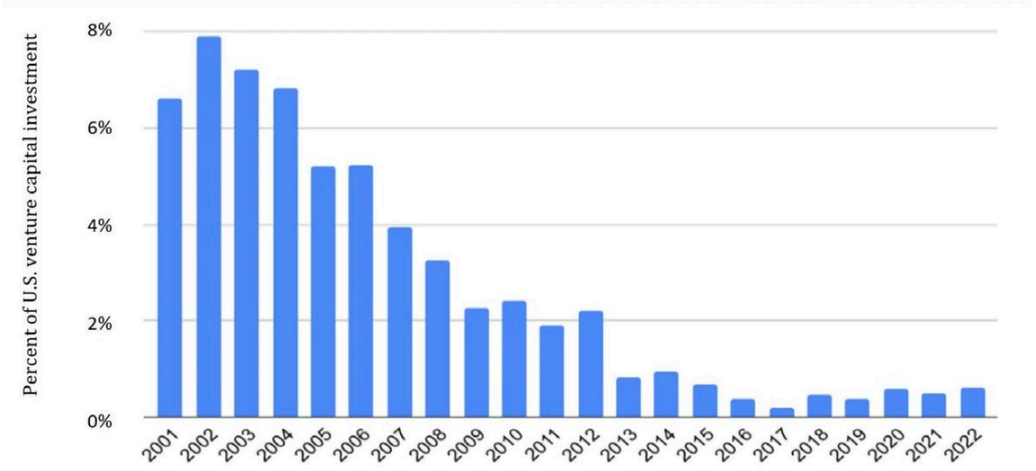


Figure 2: Percent of U.S. venture capital investment in semiconductors since 2001.
Source: Courtesy of Pear Ventures using original data retrieved from Crunchbase in August 2022.

solution companies, where there is hope for recurring revenue and perhaps that most defensible ground. Nowhere is that more clear than in life science solutions, where the market needs and opportunities are clear. We find those emergent startups very close to university research, and where academic disciplines meet, like in electronic engineering, materials science, semiconductor manufacturing technology, and molecular biology.

I have a favor to ask of you. We need more advisors with complementary life science experience, in operations, regulatory matters, and connections to venture capital. Please send us warm introductions to advisors you'd like us to engage. (group email address goes here).

Thank you all – advisors, strategic partners, in-kind partners and general well-wishers. It's been a great eight years, looking forward to exploring the future with you all, and maybe having a party or two.

SILICON CATALYST LIFE SCIENCE PORTFOLIO COMPANIES

We've been rather quietly building in those areas, and we've asked our startups in this new area to describe themselves. We hope you're as enthusiastic as we are about this added focus. We freely admit most of us are new to life sciences – these newly admitted early-stage companies in our Incubator include:

Aplife Biotech www.aplifebiotech.com - transforming health with bioelectronics

Exokeryx www.exokeryx.com - developing diagnostic solutions to revolutionize early detection of cancer and other diseases

Phinomics www.phinomics.com – defining the circulome to solve disease

APRIL 2015

STRATEGIC INVESTMENT PARTNER

MAYFIELD

Mayfield and Silicon Catalyst Form Alliance to Fuel Semiconductor Startup Innovation

Legendary venture capital firm powers renaissance of silicon

Menlo Park & San Jose, California, December 6, 2022 — Top-tier venture capital firm Mayfield and leading semiconductor incubator Silicon Catalyst today joined forces to foster startup innovation. Under the terms of their alliance, Mayfield will invest capital in and provide mentoring to seed stage companies admitted to the Silicon Catalyst Incubator/Accelerator and evaluate them for follow-on investments.

The collaboration follows Mayfield's conviction in the renaissance of silicon, a trend that has accelerated in the wake of the plateauing of Moore's Law. Over the last five years, Mayfield has partnered with the founders of Alif Semiconductor, Frore Systems, Fungible, Graphwear, NUVIA (acquired by Qualcomm), Recogni, and a couple of stealth startups. This follows the firm's 50+ year track record of investing in iconic semiconductor companies such as Cypress, Inphi, LAM Research, LSI Logic, MIPS, Qtera, S3 and Sandisk.

"It is an honor to partner with Silicon Catalyst to nurture the wave of entrepreneurs bringing silicon back to Silicon Valley," said Navin Chaddha, Mayfield Managing Partner. "The Silicon Catalyst team have been unwavering supporters of entrepreneurs across the semi ecosystem, spanning photonics, IP, MEMS, sensors, materials and life science innovation teams worldwide. They have their finger on the pulse of the major societal trends and technology inflection points that are powering this renaissance. Together, we are excited to watch many industries being revolutionized by the new wave of semiconductor startups."

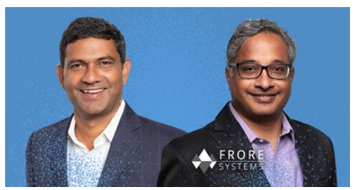
"Mayfield and Silicon Catalyst share the same goal of driving semiconductor innovation and startup company market success", stated Pete Rodriguez, Silicon Catalyst CEO. "It is exciting to know that most seed stage companies will be eligible to receive $150K at admission into the Silicon Catalyst program as a result of our alliance with Mayfield. Furthermore, this will allow startups to hit the ground running in conjunction with free shuttle runs, design tools and IP from our more than 60 in-kind partners which include TSMC, Synopsys and ARM."

As these incubated companies progress through incubation, they will be eligible to apply to Silicon Catalyst Angels and additionally receive matching investments of up to $250K per company from our new alliance. Finally, startup companies that received these investments and execute on their plans will be at the top of the pipeline for future investments through Mayfield's regular investment funds.

ABOUT MAYFIELD

Mayfield is a global venture capital firm with a people-first philosophy and a 50+ year track record of inception and early-stage investing, partnering with founders to build iconic enterprise, consumer, semiconductor, and human & planetary health companies. Since its founding, the firm has invested in more than 550 companies, resulting in 120 IPOs and more than 225 acquisitions, and currently has $2.2B under management. For more information, go to www.mayfield.com or follow @MayfieldFund.

Partnered at Series A



Partnered at Seed

Partnered at Seed

STRATEGIC PARTNER
EMD ELECTRONICS

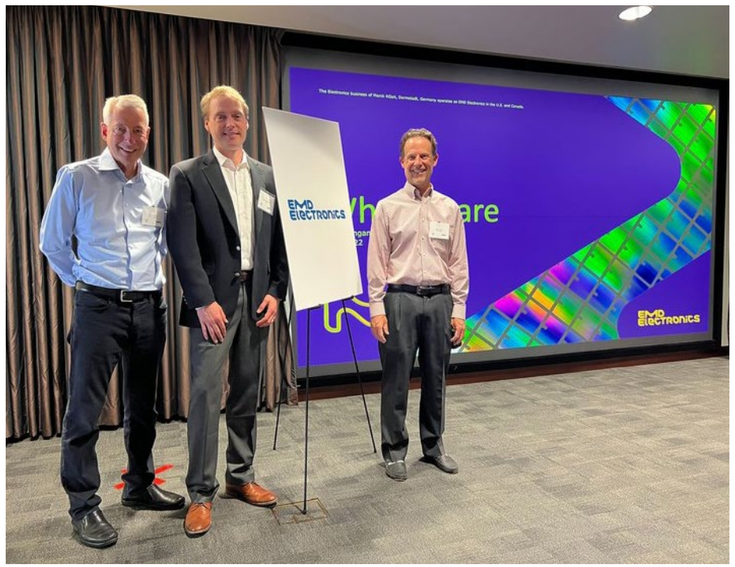
Silicon Catalyst welcomes EMD Electronics as Newest Strategic Partner

Expanding incubation for emerging electronic semiconductor material innovators

Silicon Valley, California - June 15, 2022 — Silicon Catalyst, the world's only incubator focused exclusively on accelerating solutions in silicon, announces that EMD Electronics has become its 10th Strategic Partner. In addition to EMD Electronics gaining a first-hand view of early-stage companies targeting the AI, Big Data, IoT and 5G semiconductor application markets, the companies will work together to screen and select entrepreneurial teams developing innovative electronic materials required for next-generation semiconductor devices.

EMD Electronics is the North American electronics business of Merck KGaA, Darmstadt, Germany, a leading science and technology company, operating across the life science, healthcare and electronics segments. Today, EMD Electronics has approximately 2,000 employees around the country, with regional offices in Tempe, Arizona and Philadelphia, Pennsylvania.

"We are excited about our partnership with Silicon Catalyst. By leveraging their unique incubator ecosystem, we will be able to create relationships with early-stage start-ups that are working to address critical challenges in the semiconductors and Electronics industry. We look forward to accelerating innovation through our strategic collaboration," stated Dr. John Langan, Chief Technology Officer, EMD Electronics.



Dan Armbrust, Silicon Catalyst Co-founder and Director, Dr. Jacob Woodruff, Head of Technology Scouting & Partnerships, EMD Electronics and Nick Kepler, COO, Silicon Catalyst, at the Silicon Catalyst Portfolio Company Update announcing the relationship

Silicon Catalyst has created a unique ecosystem to provide critical support to semiconductor hardware startups as they move from idea through prototype to initial product. Since its founding in 2015, Silicon Catalyst has reviewed over 600 early-stage companies and has admitted 48 startups into the incubator. These Portfolio Companies have access to tools and services from a comprehensive network of In-Kind Partners (IKPs) -- including design tools, simulation software, design services, foundry PDK accessand MPW runs, test program development and tester access -- that dramatically reduce the cost of chip development. Additionally, the startups tap into the world-class Silicon Catalyst ecosystem of advisors, investors and academic research organizations.

"Silicon Catalyst recognizes that semiconductor innovations increasingly involve the introduction of new materials and processes to enhance sensing and computing functions. We are therefore expanding the focus of our incubator beyond mainstream memory- and logic-based processes and into MEMS, sensors, photonics and semiconductor materials and processes in response to the need for electronics to interact with the world and respond locally," stated Dan Armbrust, co-founder and board director at Silicon Catalyst. "Industry stakeholders are joining Silicon Catalyst to have a early and first-hand view as to what is happening in these areas and we are growing our ecosystem to meet these needs. We welcome EMD Electronics into this ecosystem and value their insights and interest in emerging electronic materials and their use in foundry processes and next-generation devices."

SILICON STARTUP SOLUTIONS

Presentation by Dr. John Langan, Chief Technology Officer, EMD Electronics

"EMD Electronics believes in the power of collaboration to advance technology and innovation. By working with Silicon Catalyst on our outreach campaign, we will have a unique opportunity to engage with startups that share our passion for science and technology and our drive to fuel the new cycle of semiconductor innovation. The potential brought by our partnership with Silicon Catalyst is truly exciting for our electronics business," stated Dr. Jacob Woodruff, Head of Technology Scouting & Partnerships, EMD Electronics.

ABOUT EMD ELECTRONICS

Merck KGaA, Darmstadt, Germany, a leading science and technology company, operates across life science, healthcare and electronics. More than 60,000 employees work to make a positive difference to millions of people's lives every day by creating more joyful and sustainable ways to live. From advancing gene editing technologies and discovering unique ways to treat the most challenging diseases to enabling the intelligence of devices – the company is everywhere.

In 2021, Merck KGaA, Darmstadt, Germany, generated sales of € 19.7 billion in 66 countries.

The company holds the global rights to the name and trademark "Merck" internationally. The only exceptions are the United States and Canada, where the business sectors of Merck KGaA, Darmstadt, Germany, operate as MilliporeSigma in life science, EMD Serono in healthcare and EMD Electronics in electronics. Since its founding in 1668, scientific exploration and responsible entrepreneurship have been key to the company's technological and scientific advances. To this day, the founding family remains the majority owner of the publicly listed company. More information can be found at www.emdgroup.com

STRATEGIC PARTNER
NXP

NXP: Helping to make the future bright, safe, and secure

Semiconductor technologies are a crucial component empowering today's consumer and industrial applications. Whether it's tapping your phone to pay or controlling appliances with your voice, semiconductors are what make it possible for the world around us to be connected, aware, secure, and more sustainable.

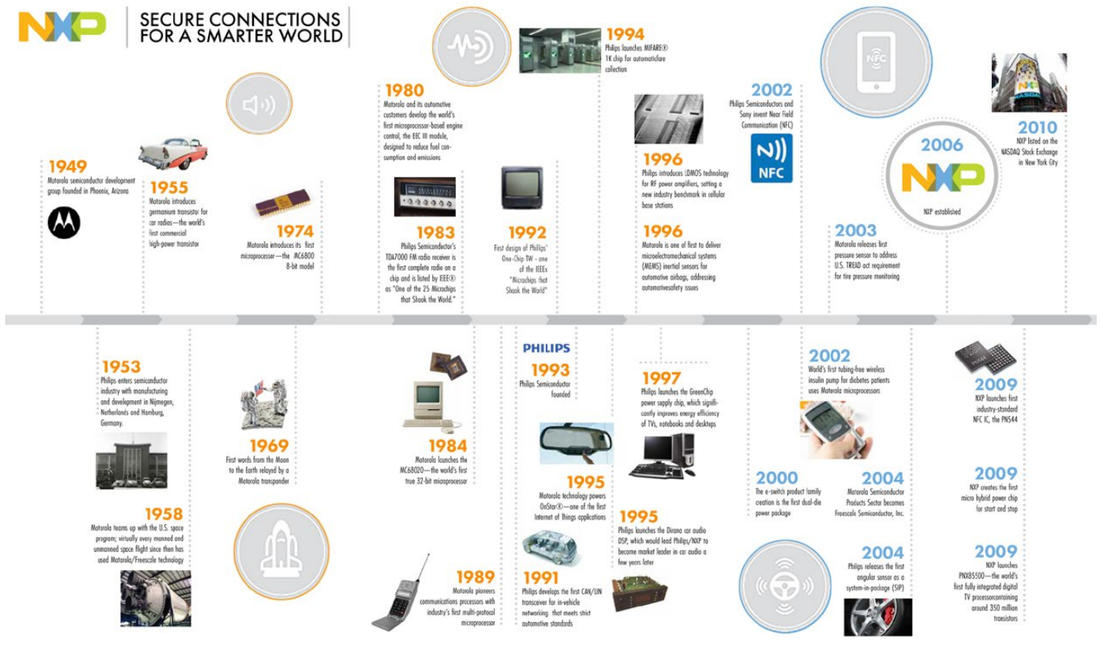
As a world leader in secure connectivity solutions for embedded applications, NXP® Semiconductors is pushing the boundaries of technology across the automotive, industrial & IoT, mobile, and communication infrastructure markets. As one of the incubator's newest strategic partners, we look forward to continuing our long history of innovation through collaborations with those in the Silicon Catalyst ecosystem across AI and machine learning, wireless, power and connectivity, among others.

LARS REGER
EXECUTIVE VICE PRESIDENT AND CHIEF TECHNOLOGY OFFICER

WHO WE WERE AND WHO WE ARE NOW

NXP, headquartered in Eindhoven, Netherlands, designs and manufactures a variety of devices used to sense, think, connect, and act intelligently to improve people's daily lives.

Formed in 2006 when Philips spun off its semiconductor operations, NXP



Semiconductors went public in 2010. Since then, we have grown organically and through acquisitions; our most significant transaction was our merger with Freescale Semiconductor in 2015.

Though NXP was founded relatively recently, our semiconductor heritage stretches back to the earliest days of the industry. Philips began exploring semiconductor materials in the 1930s and established a manufacturing facility in 1955. Freescale, meanwhile, was a spinout of Motorola, which established its semiconductor development group in 1949.

Today, NXP is a world leader in secure connectivity solutions for embedded applications. We employ approximately 31,000 people in more than 30 countries, and in 2021 reported revenue of $11 billion. The company is led by President and CEO Kurt Sievers, who started with Philips in 1995.

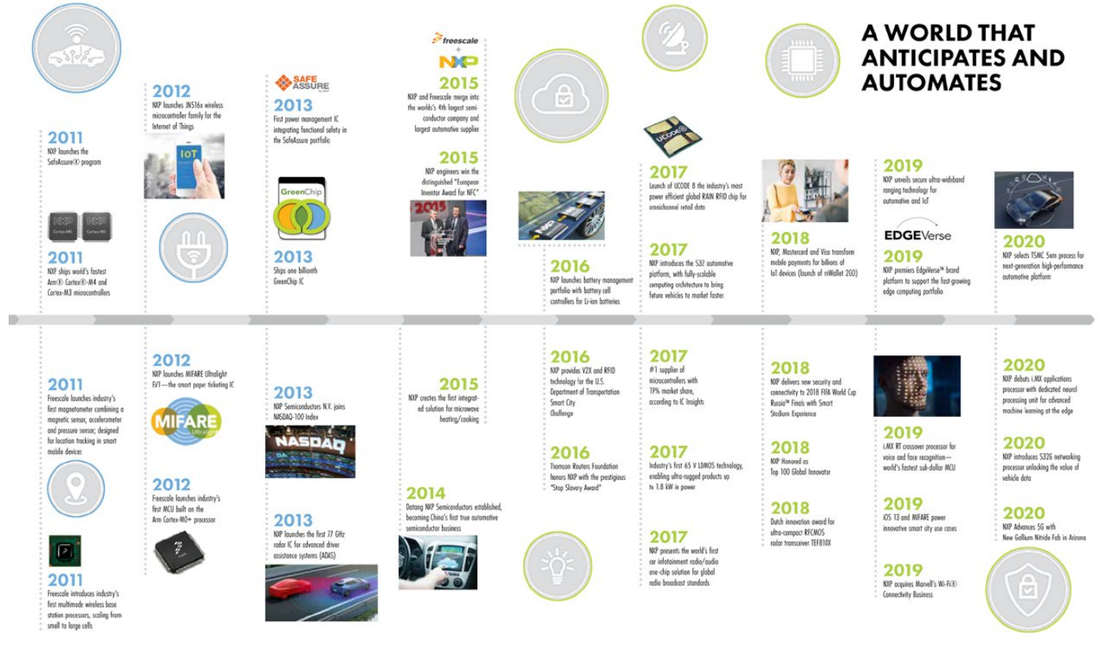
We do much of our own manufacturing, with wafer fabs in the Netherlands, the United States, and Singapore, complemented by several test and assembly plants in Southeast Asia.

A SMARTER WORLD STARTS WITH NXP

NXP has one of the most diverse and sophisticated product portfolios in the semiconductor industry, spanning embedded controllers and processors, advanced sensors, power ICs, connectivity devices, and more. Our products are designed to be reliable, safe, and secure.

Because of the breadth of our product portfolio, we are one of the few semiconductor manufacturers able to offer full system solutions.
NXP focuses on four key growth markets:

Automotive, where we provide solutions to complex autonomy, connectivity, and electrification challenges for today's safe and secure vehicles. NXP products are integral in power trains, advanced driver assist systems (ADAS), infotainment systems, vehicle-to-X communications, and more.



STRATEGIC PARTNER
NXP

Communication Infrastructure, where we support 5G-connected, edge computing technologies that support scalable communication networks.

Industrial and IoT. For industrial and IoT applications, NXP supplies simplified machine learning solutions that automate better decision-making at the device level for Industry 4.0 applications. Our portfolio of connectivity devices supports every major wireless communications protocol.

Mobile, covering both mobile devices and wearable technology, we provide solutions for connected lifestyles that involve data moving more freely and transactions that are easy, safe, and secure.

Our products are also increasingly relied on for smart home and smart city applications. We support smart home applications with solutions that listen, learn, and adapt into the places we call home for more comfort, safety, and convenience. Our smart city solutions simplify how people access and interact with local services to achieve new standards of sustainability,

efficiency, mobility, and economic growth.

THE ROAD AHEAD

NXP is poised to address what will surely be some of the biggest technological growth markets for years to come. Smart devices will become more pervasive because they help make our world richer, more fulfilling, safer and more secure, as well as more environmentally responsible. As electronics proliferate in our lives, the world will become more connected, and smarter because of it. We see that happening now with electric vehicles with ADAS features, mobile wallets, smart factories, and so much more. We look forward to working with Silicon Catalyst and its ecosystem of startups and young companies to imagine and help create what comes next.
https://siliconcatalyst.com/silicon-catalyst-welcomes-nxp-electronics-as-newest-strategic-partner

EXPERIENCE

Lars Reger is executive vice president and chief technology officer for NXP Semiconductors. As CTO, Lars is responsible for managing new business activities and R&D in the automotive, industry 4.0, internet of things (IoT), mobile, connectivity and infrastructure focus markets.

Before joining NXP as head of automotive strategy in 2008, Lars gained deep insight into the microelectronics industry with a focus on the automotive sector. He began his career with Siemens Semiconductors as a product engineer in 1997. His past roles at Infineon included head of the process and product engineering departments, project manager for mobile system chips and director of IP management. At Continental, Lars was responsible for business development and product management within the connectivity business unit.

In 2012, Lars was appointed CTO of Automotive at NXP and in December 2018, he was appointed NXP's CTO with responsibility for the overall technology portfolio.

SILICON CATALYST PARTNER
DR. ATIYE BAYMAN

Incubator expands outreach to MEMS and semiconductor materials startups

Silicon Valley, CA - August 31, 2022 — Silicon Catalyst, the world's only incubator focused exclusively on accelerating solutions in silicon, announces the appointment of Dr. Atiye Bayman as Partner. In particular, Dr. Bayman will be directly involved in the screening, selection and incubation of the entrepreneurial teams developing the next generation of MEMS devices and materials for semiconductors.

Dr. Bayman has been involved with Silicon Catalyst for the past four years, in the roles of Advisor, a Silicon Catalyst University Ambassador, and as a member of the Silicon Catalyst Angels investment group. She began her career as a process development engineer at AMD and then focused on semiconductor, technology development and transfer of technologies into production at Synergy Semiconductor and Novellus. She later moved to solar energy, where she was CTO at MiaSolé, a solar technology and products company specialized in thin film, flexible and light weight solar products. Dr. Bayman has a Ph.D. in Solid State Physics from UC Santa Barbara, California.

"I am thrilled to have Atiye expand her role with Silicon Catalyst by becoming a full partner," said Nick Kepler, COO of Silicon Catalyst. "The timing is excellent with EMD Electronics recently joining us as a Strategic Partner, as we expand further into MEMS and electronic materials. Atiye will be a major contributor as Silicon Catalyst supports early-stage companies developing innovative electronic materials and foundry processes required for these next-generation semiconductor devices."

DR. ATIYE BAYMAN
SILICON CATALYST
ADVISOR

"Going from a concept for innovation, to a prototype and then ultimately to a viable product and business requires the ability to fully understand the key challenges involved and bring to bear the appropriate expertise and direct experience. I'm extremely pleased to be stepping up my involvement with Silicon Catalyst, looking to add my experience to their comprehensive incubation process," stated Dr. Bayman.

For further background information, see Dr. Bayman's interview published in the Silicon Catalyst Newsletter, Volume 13, starting on page 60.

Silicon Catalyst has created a unique ecosystem to provide critical support to semiconductor hardware startups as they move from idea through prototype to initial product. Portfolio Companies in the incubator have access to tools and services from a comprehensive network of In-Kind Partners (IKPs) -- including design tools, simulation software, design services, foundry PDK access and MPW runs, test program development and tester access -- that dramatically reduce the cost of chip development. Additionally, the startups tap into the world-class Silicon Catalyst ecosystem of advisors, investors and academic research organizations.

ATIYE BAYMAN

Atiye Bayman has joined Silicon Catalyst as a partner after being involved with Silicon Catalyst in the roles of Advisor, a Silicon Catalyst University Ambassador, and as a member of the Silicon Catalyst Angels investment group.

She most recently served as the CTO of MiaSolé, where she led technology strategy and research and development for flexible and lightweight thin-film solar products. She continues to serve the solar industry as an advisor to Swift Solar.

Atiye's long career in Silicon Valley has been focused on semiconductor technology development for integrated circuit and products. She has developed expertise in transfer of technology and products into manufacturing as well as building and leading R&D teams. She has held various leadership positions in technology R&D at MiaSolé, Novellus Systems, Synergy Semiconductor (acquired by Micrel), and Advanced Micro Devices.

Atiye holds a Ph.D. in solid state physics from the University of California, Santa Barbara, and a Bachelor of Science in Physics from Middle East Technical University in Ankara, Turkey.

INDUSTRY PARTNER
LUMINATE

Luminate and Silicon Catalyst form partnership to speed development of emerging technologies

Collaboration will improve chip design and development to de-risk early-stage investments

ROCHESTER, New York, Silicon Valley, November 14, 2022 — Luminate NY—the world's largest accelerator for startups developing optics, photonics, and imaging (OPI) enabled technologies—announced today that it has formed a strategic partnership with Silicon Catalyst, the world's only incubator plus accelerator focused on semiconductor solutions. Under the joint partnership, the two organizations will work closely together to recruit the most innovative early-stage startups into their accelerator programs to allow for concurrent participation. This will expand the support ecosystem for founders working on industry solutions that are enabled by OPI and semiconductor chip design to ultimately reduce the cost and complexity of development. Companies developing OPI-based products accepted into the accelerator will be eligible to receive funding of up to $2 million to support their business plans.

"Critical technologies such as silicon photonics, lasers, and electronic packaging rely on the integration of semiconductor technology and photonics. These complex integrations are the building blocks of emerging applications like autonomous sensing, augmented reality, artificial intelligence, and quantum applications," said Sujatha Ramanujan, Managing Director, Luminate NY. "This partnership will help to close the development and manufacturing gaps that often exist when working across multiple technical disciplines to bring novel technologies to market."

Owl Autonomous Imaging, (www.owlai.us) an early-stage company that graduated from the Silicon Catalyst Incubator, experienced this problem firsthand when it needed to integrate optics and imaging with machine learning and silicon chip design in order to deliver the first monocular 3D Thermal Ranging solution to the autonomous vehicle industry. Owl first earned a spot in Silicon Catalyst's 24-month accelerator in 2018. In 2021, it was accepted into Luminate's fourth cohort. During this time period, the company had to execute on a very aggressive schedule for chip-level development, while at the same time, build a complete imaging automotive-grade system solution. Additionally, New York Governor Kathy Hochul announced in July of this year that Owl will expand its operations in Monroe County in the Town of Perinton, committing to creating up to 105 high-technology jobs in the region. The project will see the autonomous imaging company move into a larger facility located at the Willowbrook Office Park.

"No one incubator brought to bear world class expertise across all the varied technical disciplines required for our success," said Gene Petilli, Co-founder and Chief Technology Officer, Owl Autonomous Imaging. "Working together with both Silicon Catalyst and Luminate, we were able to leverage their strategic and in-kind partners, financiers, advisors, and mentors to build a solid company foundation and, ultimately, introduce a world-first solution."

Owl's patented 3D Thermal Ranger™ provides HD imaging and precision ranging, which represents a 150x improvement in resolution and cloud density of LiDAR. It operates both day and night, in all weather, to definitively classify pedestrians, cyclists, animals, and vehicles, all the while calculating position, direction, and speed to unlock safe autonomous and semi-autonomous operation.

"Owl's success helped Silicon Catalyst and Luminate validate the impact that a strategic partnership could have on the development trajectory of groundbreaking technologies," said Pete Rodriguez, CEO, Silicon Catalyst. "By formalizing this relationship and working together, we'll be able to more effectively screen and evaluate each startup's potential, closely pair our cohort companies to mentors and resources to speed time to market, and de-risk investments.

In addition to providing the ability to participate in both accelerators concurrently, the partnership will increase startup access to connections, collaborations, and funding. Luminate and Silicon Catalyst will collaborate on startup recruitment and selection, with a focus on elevating women and minority owned companies to ensure equitable access to comprehensive support. The organizations will also leverage their investor networks and portfolios to improve funding opportunities.

Silicon Catalyst provides critical support to semiconductor hardware startups as they move from idea through prototype to initial product. Since its founding in 2015, it has reviewed over 700 early-stage companies and admitted 88 startups into its incubator. The companies get access to tools and services from a comprehensive network of In-Kind Partners (IKPs)—including design tools, simulation software, design services, foundry PDK access and MPW runs, test program development, and tester access—which dramatically reduces the cost of chip development. Additionally, the startups tap into the world-class Silicon Catalyst ecosystem of advisors, investors and academic research organizations. In 2021, Silicon Catalyst was named Semiconductor Review's Top-10 Solutions Company award winner.

Since its inception in 2018, Luminate has reviewed more than 500 early-stage companies from around the world for entrance into its competitive, six-month accelerator program, and has accepted and invested $15 million in 53 startups. The companies in the portfolio now share a net worth of over $400 million, and many are establishing U.S. operations or some aspect of research and manufacturing in the Rochester and Finger Lakes New York region, which has long been viewed as the optics and imaging capital of the world.

Luminate is now recruiting for Cohort 6. Startups interested in applying are encouraged to register for an upcoming information session, or apply by Jan. 9, 2023.

The strategic partnership dovetails on recent news that highlights New York's deepening commitment to both OPI and semiconductor capabilities, which includes funding for Luminate for four more years from Empire State Development's Finger Lakes Forward Upstate Revitalization Initiative, and Micron's plans to invest $100 billion transform Central NY into a global, leading-edge semiconductor manufacturing hub.

ABOUT LUMINATE

The Luminate NY accelerator is based in Rochester, New York, and selects ten promising companies each year to participate in its six-month program. During this time, companies are provided with comprehensive training and resources to advance their technologies and businesses. Applications are now being accepted for Round 6 through January 9, 2023. Teams that can physically locate to Rochester will receive $100,000 in funding upon program start in April 2023. Teams that are unable to come to Rochester due to travel and Visa restrictions will receive $50,000 in funding upon program start and an additional $50,000 that must be used to engage resources in the Finger Lakes region during their time in the accelerator. For more information on Luminate NY, visit: https://luminate.org/.

CHIPS FOR AMERICA
NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

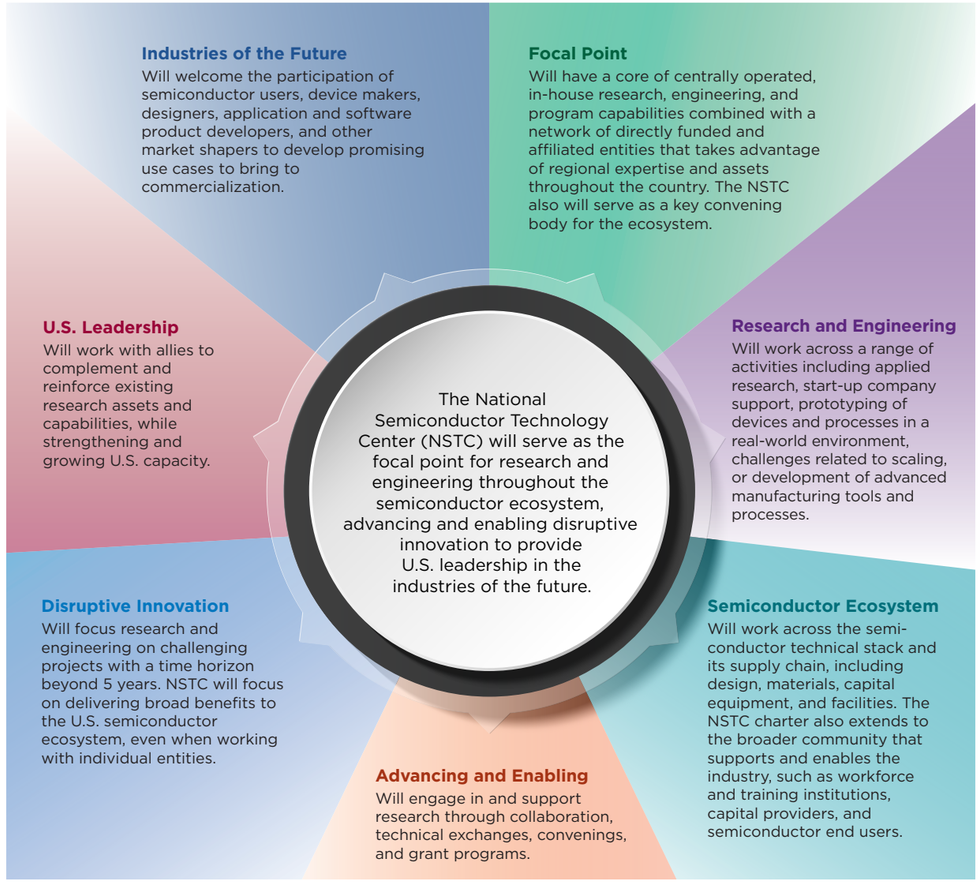
CHIPS Research and Development Office Nov. 16, 2022

INTRODUCTION

The CHIPS for America initiative will invest $50 billion to supercharge the U.S. semiconductor industry and revitalize our innovation ecosystem. This funding includes $11 billion for research and development—the focal point of which will be the National Semiconductor Technology Center (NSTC), an innovation hub that will advance semiconductor technology and seed new industries built on the capabilities of a wide range of advanced chips.

The NSTC will be a public-private consortium that provides a platform where government, industry, customers, suppliers, educational institutions, entrepreneurs, workforce representatives, and investors converge to address the semiconductor ecosystem's most pressing challenges and opportunities.

National Semiconductor Technology Center Mission



SILICON STARTUP SOLUTIONS

CHIPS FOR AMERICA
NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

Using a whole-of-government approach, and as specified by statute,* the NSTC will develop a comprehensive semiconductor research and development program that will include research, prototyping capabilities, an investment fund, and workforce development programs.

NSTC STRUCTURE

The NSTC will be a public-private consortium, as required by statute. The Department of Commerce (the "Department") anticipates the creation of an independent entity with NSTC leadership reporting to a governing board informed and advised by industry, academia, government, and key stakeholders. The U.S. government is developing further guidance regarding the governance structure but anticipates a structure that includes public interest directors both to ensure that public objectives are met and to provide accountability for spending taxpayer funds.

NSTC DEFINITION PROCESS

To inform the development of the NSTC, the Department has conducted and continues to conduct significant stakeholder engagement. The Department received more than 250 responses to a request for information (RFI) that included questions on the scope of the NSTC. Responses represented input from different sectors of the semiconductor supply chain including design software developers; integrated device manufacturers; materials suppliers and equipment vendors; fabless, automotive, industrial, and consumer companies; and academic institutions and organizations representing labor. In alignment with the RFI, the Department hosted 26 workshops and listening sessions with different parts of the semiconductor value chain. Two workshops specifically focused on the NSTC and the National Advanced Packaging and Manufacturing Program, drawing a combined 350 registrants. The Department also is considering the recommendations from the President's Council of Advisors on Science and Technology, public reports like one recently published by the Semiconductor Industry Association, and input from potential partners. The Department will continue to reach out to interested members of the community as plans are developed.

* 15 U.S.C. § 4656(c).

At present, the Department is engaged in four high-priority tasks:

1. Evaluating potential gaps in research and engineering that could be filled by the NSTC. As part of the whole-of-government effort, the NSTC will complement the many excellent centers already established by industry, academia, allies, and other governmental agencies. The Department will create a preliminary landscape analysis with the benefit of recommendations developed by the CHIPS Industrial Advisory Committee. Ultimately, the NSTC itself will finalize the focus areas, but this early work will inform further decisions.
2. Evaluating and defining a structure and governance model that fulfills the CHIPS for America goals of promoting U.S. economic and national security and protecting taxpayer investments while ensuring technical excellence and leadership.
3. Creating a preliminary operating, business, and financial model that will serve as a road map for near-term investment informed by an understanding of what will be required for long-term sustainability.
4. Identifying a slate of candidates for the NSTC chief executive.

The Department will release a white paper in the first quarter of 2023 that will summarize the results of the landscape analysis, governance structure, and preliminary operating and financial model. At that time, the Department will issue guidance on when to expect requests for proposals.

CONCLUSION

The Biden-Harris Administration and a bipartisan group in Congress made the bold decision to establish a new and important public-private consortium that will benefit the country for generations to come. The Department will invest taxpayer funds deliberately and effectively to ensure the greatest potential impact for the U.S. economy and national security, and looks forward to working with the broader community to achieve this objective.

Portfolio Companies

CURRENT

EXOKERYX

POLYN TECHNOLOGY
NEUROMORPHIC ANALOG SIGNAL PROCESSING

XCELERIUM

QPT

Zepsor

cellsemi

KURA

Siloxit

Lemurian Labs

RAAAM
The Highest Density On-Chip Memory in Standard CMOS

PHINOMICS

plife
BIOTECH

NanoHydroChem
Energy Storage Solutions

SALIENCE LABS

ALPHA ICs
ADVANCING AI COMPUTE

Lelantos

SONICAL

MultiFractal
SEMICONDUCTORS

SigmaSense

Smarter EH PMICs
Trameto

ESPRE TECHNOLOGIES

MENTIUM
TECHNOLOGIES

GEEGAH

FORUM5

SEMICONDUCTOR INDUSTRY FORUM

"2023: Welcome to the Danger Zone" Survive or Thrive?

Silicon Catalyst is pleased to continue our collaboration with Silicon Valley Bank in hosting our 5th Annual Semiconductor Industry Forum, returning to an in-person event on December 6 at their auditorium in Santa Clara.

The Silicon Catalyst Semiconductor Industry Forum was launched in 2018, hosted at the TSMC Silicon Valley headquarters. The Forum's charter is to enable a town-hall like event to discuss the broad impact of semiconductors on our world, beyond the traditional focus on technology and financial reviews and forecasts.

The topics discussed during that inaugural 2018 event covered the cost of fabs, IoT business opportunities, memory technology and foreshadowed the gathering storm clouds about the potential impact of China's activities in the semiconductor sector. Clearly, the key take-away was that the semiconductor industry was on the verge of major structural changes.

Looking back now as we close out 2022, wow, was that an understatement!

For a re-cap of the 2018 Forum, check out the IEEE Spectrum coverage at https://spectrum.ieee.org/semiconductor-industry-veterans-see-the-old-order-crumbling.

Zoom recordings of Forum 3 2020 and Forum 4 2021 are available for replay from our website.

FORUM5 - "2023: WELCOME TO THE DANGER ZONE"

The coming year is shaping up as the perfect storm for our industry, as we look to adapt to the unprecedented challenges to be addressed across our businesses, along with our personal and national security. We've arranged a stellar panel of speakers, moderated by Don Clark, contributing journalist for the NY Times for our Forum5 event.

Silicon Catalyst CEO, Pete Rodriguez, will kick things off with an insider's view of his participation on the PCAST Semiconductor Working Group and the creation of the report to the President. For background information about the PCAST Group, I encourage you to read the details at:

WhiteHouse.gov

The Full Report

NIST

The Forum5 panel will discuss potential strategies and tactics to help us navigate through the danger zone and includes:

SILICON STARTUP SOLUTIONS

Navin Chaddha – Managing Director, Mayfield Fund

Navin is Managing Director at Mayfield. He has been named a Young Global Leader by the World Economic Forum and has ranked on the Forbes Midas List of Top 100 Tech Investors fourteen times, including being named in the Top Five in 2020 and 2022. His investments have created over $120 billion in equity value and over 40,000 jobs. During his venture capital career, Navin has invested in over 60 companies, of which 18 have gone public and 25 have been acquired. He believes the Renaissance of Silicon will create industry giants and has invested in semiconductor companies including Nuvia, Fungible, Alif Semiconductor, Frore Systems, and several others in stealth. As an entrepreneur, Navin has co-founded or led three startups, of which one went public and 2 were acquired. Navin holds an MS degree in electrical engineering from Stanford University and a B.Tech. degree in electrical engineering from IIT Delhi, where he was honored with a distinguished IIT Alumni Award.

Dr. Walden Rhines, President & CEO of Cornami; GSA 2021 Morris Chang Exemplary Leadership award recipient

Dr. Rhines is President and CEO of Cornami, Inc., a fabless software/semiconductor company focused on intelligent computing for fully homomorphic encryption and machine learning. He was previously CEO of Mentor Graphics for 25 years and Chairman of the Board for 17 years. During his tenure at Mentor, revenue nearly quadrupled and market value of the company increased 10X. Prior to joining Mentor Graphics, Dr. Rhines was Executive Vice President, Semiconductor Group, responsible for TI's worldwide semiconductor business. Dr. Rhines has served on the boards of Cirrus Logic, QORVO, TriQuint Semiconductor, Global Logic, PTK Corp. and as Chairman of the Electronic Design Automation Consortium (five two-year terms). He is a Lifetime Fellow of the IEEE. Additionally, his experience includes four years on the board of SEMATECH, three years on the board of SEMI-SEMATECH and twenty years on the board of SRC (Semiconductor Research Corporation). Dr. Rhines holds a Bachelor of Science degree in engineering from the University of Michigan, a Master of Science and PhD in materials science and engineering from Stanford University, an MBA from Southern Methodist University and Honorary Doctor of Technology degrees from the University of Florida and Nottingham Trent University.

Maryam Rofougaran – CEO and Founder, Movandi

Maryam Rofougaran is founder and CEO of Movandi, a leader in new 5G RF and millimeter wave technology that is commercializing multi-gigabit, 5G millimeter wave networks. Movandi is breaking through coverage and network challenges of 5G millimeter wave networks. Their BeamXR active repeater and system solutions solves today's real world 5G deployment challenges – by increasing 5G coverage and capacity, while reducing infrastructure costs by 50%, accelerating large-scale 5G commercialization. Prior to co-founding Movandi, Maryam was the Sr Vice president of Radio Engineering at Broadcom and was instrumental in starting and building the wireless business at Broadcom and in growing it to annual revenues of more than $3 billion. She is an Inventor and co-inventor on 300 U.S. issued patents, 85 U.S. filed patents and is co-author to many publications. Her first startup, Innovent Systems was acquired by Broadcom Corporation and was the entrance of Broadcom in wireless business.

Mark Edelstone from Forum 4.0. Chairman,
Global Semiconductor Investment Banking, Morgan Stanley

PORTFOLIO COMPANY NEWS
A WEBINAR

THE SILICON CATALYST THOUGHT LEADERSHIP SERIES

"How Safe Are We with Today's ADAS?"

A Silicon Catalyst Thought Leadership Webinar Series Hosted in Collaboration with The Ojo-Yoshida Report

Talking safety is easy. Claiming safer vehicles is a breeze if you don't have to back your boasts with proof. SAE levels are product categories, not evidence of any degree of safety.

In this webinar, we share candid insights from leading thinkers and tech developers in a quest to establish clearly where the auto industry stands with sensing technologies and the perception hardware/software stack, as it relates to both driver and pedestrian safety. One of today's key technology issues is whether carmakers can honestly tell consumers: "We've got you covered." If this isn't quite so, what is still missing?

Bolaji and Yoshida have decades of experience working at leading publications, covering automotive technology – with safety as their foremost emphasis. Today, The Ojo-Yoshida Report is an independent platform, without favorites or hidden agendas. This inaugural webinar will offer a comprehensive, up-to-the-minute understanding of today's safety and automation landscape.

https://siliconcatalyst.com/sicoy-report-thought-leadership-webinar-news

ILLUSTRIOUS PANELISTS:

MODERATORS:

Junko Yoshida, Editor-in-Chief of The Ojo-Yoshida Report

Bolaji Ojo, Publisher & Managing Editor of The Ojo-Yoshida Report

PANELISTS:

Matthew Lum, Engineering Program Manager, AAA National

David Aylor, Vice President of Active Safety Testing, The Insurance Institute for Highway Safety (IIHS)

Jordan Greene, Co-Founder, GM of Automotive & VP of Corporate Development, AEye, Inc.

Chuck Gershman, President & CEO, Owl Autonomous Imaging, Inc

Patrick Denny, Lecturer in Artificial Intelligence and Industry Expert in Automotive Imaging, Univ. of Limerick

Manju Hegde, CEO & Co-founder, Uhnder, Inc.

sponsored by Imagination

THE OJO-YOSHIDA REPORT
TECHNOLOGY IN CONTEXT

Junko Yoshida, Editor-in-Chief of The Ojo-Yoshida Report

SILICON STARTUP SOLUTIONS

PORTFOLIO COMPANY NEWS
A WEBINAR

THE SILICON CATALYST THOUGHT LEADERSHIP SERIES

"From AR/VR to Metaverse"

A Silicon Catalyst Thought Leadership Webinar Series Hosted in Collaboration with The Ojo-Yoshida Report

The latest McKinsey research shows that the metaverse has the potential to generate up to $5 trillion in value by 2030. It's an opportunity too big to ignore.

The Metaverse may be the next "Big Thing" of the information age. It has sparked controversies and a bucketload of questions, amongst them: what exactly is the Metaverse; what are its components; how do Augmented Reality and Virtual Reality play into it; what are the potential applications; who will drive its adoption and how will it impact business and social lives?

Silicon Catalyst in conjunction with the Ojo-Yoshida Report assembled a panel of experts to offer insights into the Metaverse and help answer questions on the minds of observers and the potential early adopters. Join our next Thought Leadership Webinar on Wednesday, October 5, 2022, for an engaging focus on the Metaverse and AR/VR.

https://siliconcatalyst.com/thought-leadership-pt-2-the-metaverse

ILLUSTRIOUS PANELISTS:

MODERATORS:

Junko Yoshida, Editor-in-Chief of The Ojo-Yoshida Report

Bolaji Ojo, Publisher & Managing Editor of The Ojo-Yoshida Report

PANELISTS:

Kelly Peng, CEO of Kura Technologies - Developer of an augmented reality system designed to build the next generation AR optics and display modules

DP Prakash, an IBM and GlobalFoundries veteran and co-CEO of the innovation startup Youtopian

Neil Trevett, vice president, developer ecosystems at Nvidia, and chair of Metaverse Standards Forum

sponsored by Imagination

THE OJO-YOSHIDA REPORT
TECHNOLOGY IN CONTEXT

Bolaji Ojo, Publisher & Managing Editor of The Ojo-Yoshida Report

SILICON CATALYST ADVISOR INTERVIEW

Jem Davies, Former VP of Technology at Arm

November 2, 2022 - Watch the full interview here.

Silicon Catalyst UK Managing Partner Sean Redmond had an opportunity to interview Jem Davies, a Silicon Catalyst Advisor. Jem is an experienced entrepreneurial senior leader, with a successful track record identifying technical trends, spotting commercial disruptions, setting strategy, and building/developing leadership teams to achieve real commercial business growth, acquiring startups to accelerate that growth, when appropriate. He has more than two decades' experience in the semiconductor and IP businesses working closely with the largest technology companies in Asia, US and Europe.

Originally an OS kernel hacker, Jem strayed across into hardware architecture and held various roles at Arm over a long career, including Fellow, VP of technology, setting technology strategy and roadmaps, finally as general manager of two startup businesses he founded/created inside Arm: media processing (producing the world's #1 shipping GPU) and AI/Machine Learning.

Based in Cambridge, UK, Jem holds four patents in the fields of CPU/GPU architecture, memory systems and compression and a degree from the University of Cambridge.

What follows is a brief sampling Sean's conversation with Dave. You can view or listen to the full interview from the Silicon Catalyst website, https://siliconcatalyst.com/advisor-ecosystem

SR: WHAT GOT YOU STARTED WITH THE SEMICONDUCTOR INDUSTRY, YOUR SCHOOLING AND FIRST JOB?

JD: I never intended actually from the start to get involved in semiconductors. I went to University to read maths. I changed and became a theoretical chemist, which was absolutely useless as a vocational qualification, and I thought I better get a job. And so I ended up in software, moving progressively further and further towards hardware until basically I was a hardware architect. I started working with semiconductors, running a small software consultancy and we were working with Arm. I then joined Arm and stepped into semiconductors full-time. My job initially was to Port Linux to the first cache coherent multi-processor that Arm was producing and I thought that was a software job.

How little did I understand that actually it was all about fixing the hardware and making sure that the hardware understood that it was there to run software and not the other way around. In my career, I've gotten involved in a number of acquisitions and even more investigations of companies not to be acquired while I was working at Arm. We were looking at buying small startups. And that's actually kind of what I am. I'm a startup guy. I built two businesses inside Arm.

SR: WHAT ADVICE WOULD YOU HAVE FOR EARLY-STAGE SEMICONDUCTOR START-UPS?

JD: The advice I would give my younger self would be about communications, about persuading people. Particularly when you're young you think you've got all the answers and you're right and everyone else is wrong. And if they don't understand that you're right, then they're stupid. And actually no, it's standard communications theory, the responsibility is on the transmitter to ensure the message gets across - it's not the responsibility of the receiver and if they don't understand you or they do something stupid because they don't understand you - it's your fault!

And even if you want to be a technical leader, as opposed to a manager, you have to work on those skills. You have to work on understanding people, making sure those people understand you and the message you're trying to get across. Having a really clever invention isn't the same as having a really good business proposition.

One of the things I really enjoy working with Silicon Catalyst is taking these very, very technical startups and say that's really clever, but that's not that's not a business proposition. So what is the problem?

From the customer's perspective, what of their problems will be solved by your clever invention. I don't care whether you call it marketing or you call it technical communication, but you've got to be able to do that. The very best startups combine that technical cleverness or invention with the ability to clearly communicate your value to the market.

I think that messaging is incredibly important and I'm convinced that communicating what it is you do is incredibly important. I understand that a lot of very technical people are allergic to the word marketing or brand or tagline, but actually the naming of things does matter.

SR: WHAT APPLICATION AREAS AND TECHNOLOGIES DO YOU SEE THAT WILL DRIVE THE NEXT BUSINESS GROWTH STAGE FOR THE SEMICONDUCTOR INDUSTRY?

JD: I wouldn't like to say I've got the exact prediction correct as to what the next big thing is, but I've got a framework within which I can see what sort of things are coming. With all due respect for my incredibly clever CPU architect colleagues, they're running out of road. You can only make your general-purpose CPUs so fast, so efficient, so low power, so high performance, you know, you can improve the memory interface. But you know, there's the end of the road is out there.

Today's computing workloads are not generic, they're not all the same thing. And so there are certain workloads, which we see have become worthwhile in building special purpose processes For graphics, obviously, you can't do 3D graphics on a CPU, it would go one frame per fortnight. You just can't do it.

What's interesting now is we're seeing other new workloads that are becoming so prominent, so prevalent that it is now worth getting special purpose processors, especially for machine learning. It's going to be huge and some people predict that you know, 50% of all compute cycles in a few years' time will be spent executing machine learning workloads. And so designing processors dedicated to those special purpose workloads will be key.

What's the next thing? There are some people I've talked to who think that data analytics and graph analytics of results from huge scale data collection activities is an important growth opportunity. The type of computation requires traversing these data structures that graph like data structures is sufficiently different than a general purpose CPU, which doesn't do it terribly well.

Watch Jem Davies speak about Arm Flexible Access (AFA) here on SiliconCatalyst.com.

JEM DAVIES

Jem is currently a non-executive director and advisor to several startup companies in the UK and US, looking for opportunities to use his expertise to achieve wider impact and success.

An experienced entrepreneurial senior leader, with successful track record identifying technical trends, spotting commercial disruptions, setting strategy, and building/developing leadership teams to achieve real commercial business growth, acquiring startups to accelerate that growth, when appropriate. More than two decades' experience in the semiconductor and IP businesses working closely with the largest technology companies in Asia, US and Europe.

Originally an OS kernel hacker, Jem strayed across into hardware architecture and held various roles at Arm over a long career, including Fellow, VP of technology, setting technology strategy and roadmaps, finally as general manager of two startup businesses he founded/created inside Arm: media processing (producing the world's #1 shipping GPU) and AI/Machine Learning.

Based in Cambridge, UK, Jem holds four patents in the fields of CPU/GPU architecture, memory systems and compression and a degree from the University of Cambridge. He enjoys gliding, diving and fireworks.

SILICON CATALYST ADVISOR INTERVIEW

Dave Dwelley, Former CTO of Maxim Integrated

October 23, 2022 - Watch the full interview here.

Managing Partner Tarun Verma had an opportunity to interview Dave Dwelley, a Silicon Catalyst Advisor. Dave was most recently CTO for Maxim, and previously spent 28 years at Linear Technology. Starting as an FAE, he transitioned from IC designer, to managing world-wide design teams in Singapore, Santa Barbara and Munich. Dave holds a Cal Berkeley BSEE degree.

What follows is a brief sampling of the conversation with Dave. You can view or listen to the full interview from the Silicon Catalyst website,

TV: WHAT GOT YOU STARTED WITH THE SEMICONDUCTOR INDUSTRY, YOUR SCHOOLING AND FIRST JOB?
DD: I got into electronics very young, somebody in my family gave me a Christmas present of one of these old Radio Shack electronic kit things with little springs that you stick the wire into and I remember thinking hey, wow, this is really cool.

I ended up going to UC Berkeley for an Electronics Engineering EECS degree. And I remember signing up at Berkeley, you had to declare your major when you when you came in on entry if you're an engineer and I remember signing up for classes my freshman year. I noticed in the electrical engineering department there were two tables - there was the digital engineering sign up which I thought was kind of cool. There was an analog engineering program. This is back in the Stone Age when they still taught analog in school. I noticed the line in front of the analog table was much, much shorter and I thought to myself, you know, it's better to be a big fish in a small pond, then a medium-sized fish in a really big pond. So I lined up on the analog side.

I graduated and took a job as an analog circuit designer at a little company in Santa Barbara, California that made a sonar system as a subcontractor to the Navy and I was the principal analog designer. I remember a couple of really interesting experiences where something would fail in the field and some Admiral would say "darn it! put the engineer on the boat next time so we can diagnose the problem. And that would be me."

TV: WHAT ADVICE WOULD YOU HAVE FOR EARLY-STAGE SEMICONDUCTOR START-UPS?
DD: Over the course of my career, I've seen a lot of the different aspects of what make semiconductor companies work. There's obviously engineering at a very high level. There's manufacturing that goes along with that engineering at a very high level, but there's customer interface and product definition, project management and sales, marketing, ops, and finance. Startups really need to be deliberate about focusing on what the company does really well, where do we really differentiate ourselves and then doubling down on that stuff.

TV: WHAT APPLICATION AREAS AND TECHNOLOGIES DO YOU SEE THAT WILL DRIVE THE NEXT BUSINESS GROWTH STAGE FOR THE SEMICONDUCTOR INDUSTRY?
DD: I'll generically call it "directed communications" in a situation where radio bandwidth comes at a premium. And if you can use spatial narrowing, basically, beam steering or sectored antennas, to take advantage of the bandwidth that's already there - by only focusing the energy or focusing the sensitivity on the place that we believe, or we know that the signal is coming from - as opposed to just blasting out signal everywhere, creating signal to noise ratios problems for everybody else in the neighborhood. I think that's something that is not flashy but critically important for the 5G system roll out, which can take great advantage of that spatial diversity. I like seeing directional comms move forward, as I think that brings real benefits because it takes a scarce resource, in this case bandwidth, and makes absolutely the best use of it.

SiliconCatalyst.UK:
it all happens here®

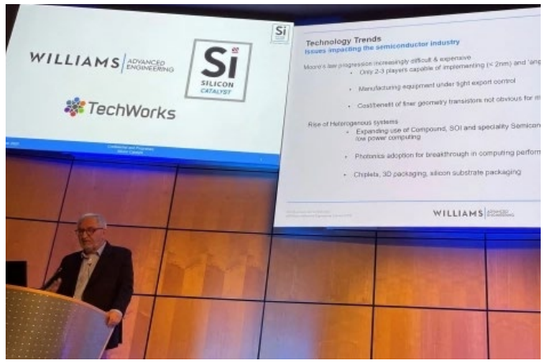
Fabless Companies Can Expect to Regain Leverage as Capacity Grows

At Silicon Catalyst semiconductor startup event at Williams Advanced Engineering, ex-Dialog CEO says good times ahead for fabless companies.

Nitin Dahad | Editor-in-Chief | Correspondent | EE Times, EE Times Europe

The next few years could be a good period for fabless semiconductor companies, especially with the expected growth in fab capacity meaning fabs will need to fill their production lines. That's the view of seasoned electronics industry executive Jalal Bagherli, speaking at this week's Silicon Catalyst semiconductor startup event at Williams Advanced Engineering in the U.K.

Bagherli, previously CEO of Dialog Semiconductor and now investor and board member at various companies, outlined the trends impacting the semiconductor industry, which center around four key areas: geopolitics, Covid-19, climate change, and the semiconductor down cycle. He said the various chips acts around the world are likely to result in over-capacity in the near future. As a result of this and the coming down cycle, he commented, "This means the fabless business model regains leverage. They [the fabs] will be desperate for your business, and silicon cost will go down."



Jalal Bagherli highlights some of the key technology trends impacting the semiconductor industry. (Images: Nitin Dahad)

Since selling Dialog Semiconductor, Bagherli has been a prolific 'commentator' on key events and trends in the semiconductor industry. In addition to the geopolitical aspect of how the industry is being impacted, in his talk he offered his perspectives about changing technology trends and business models.

JALAL TECH TRENDS

Jalal Bagherli highlights some of the key technology trends impacting the semiconductor industry. (Image: Nitin Dahad)

Since the focus of the event was on startups, he also offered his advice to startups:

- If you are fundraising, close as soon as possible and raise as much as you can – at least for a runway of 18 months before next funding round
- Stay away from 'bleeding edge' digital products – differentiate away from this to have a higher chance of success with less funding
- Focus on customer design-wins that will help create a demand pipeline for the next upturn which could be at least nine months away
- Look at opportunities created by strategic insourcing by system houses – as companies bring chip design in house, they may not have all the expertise needed which creates custom opportunities for niche and mixed signal products to complement their own processors.

Bagherli is currently co-chair at Williams Advanced Engineering (WAE), an adviser to Silicon Catalyst in the U.K., chair of ATE test hardware firm PTSL (who just this week acquired Dallas, Texas-based ThinkMEMS and also last month closed a $30 million investment from Tikehau Capital), and an investor in Salience Labs. The WAE grounds, with its Formula 1 racing history, provided the backdrop to this latest in Silicon Catalyst's series of "Forming, storming, norming & performing of semiconductor startups" events (the last one was held at Arm headquarters in Cambridge, U.K.).

SILICON STARTUP SOLUTIONS

IT TAKES TEAMWORK TO GET A NEW CHIP TO MARKET

The Silicon Catalyst event included some fascinating insight into Williams Advanced Engineering's work on electrification and battery management, followed by presentations from startups Oxford RF Solutions, Salience Labs, and QPT.

OXFORD RF SOLUTIONS

Kashiff Siddiq, founder & CEO of Oxford RF Solutions, talked about his startup's next generation ADAS sensors, which could potentially reduce the number of sensors in the car.

SALIENCE LABS

Vaysh Kewada, co-founder & CEO of Salience Labs, gives an update on the company's photonic solution for AI inference.

We also heard the journey of PTSL, from kitchen worktop with no debt or equity and just £4k of founders' capital, to finally raising external $30 million of funding this year for next phase growth.

PTSL

Jordan Mackellar, founder & CEO of Probe Test Solutions (PTSL), talked about his startup journey, including the use of a vacuum cleaner providing suction for the wafer on the kitchen top for its first test rig.

In addition, the fund manager for WAE's technology investment group, Foresight, also highlighted its work with deep tech startups, with which it gets involved at seed funding stage.

JOE JONES - WILLIAMS ADVANCED ENGINEERING

Joe Jones, product manager for battery technologies at Williams Advanced Engineering, delivered a fascinating insight to the work on battery management, battery intelligence and battery digital twins that is helping the path to electrification in many industries.

The event also presented the importance of the ecosystem and teamwork in getting a chip to market. Raspberry Pi's chief operating officer, James Adams, talked about the work involved in developing its own microcontroller (MCU), the RP2040. He said, "Making chips is hard," as he described how it took teamwork together with Arm and imec and three years to get from design to end product.

RASPBERRY PI MAKING CHIPS IS HARD

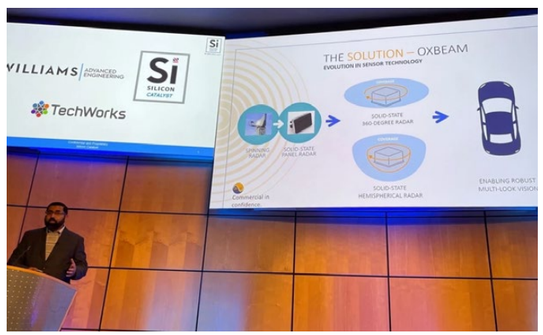
James Adams of Raspberry Pi talked about their journey to getting their own MCU to market, from design to production volume.

He said, "We had a great bootstrap with Arm flexible access and imec. It's been a team effort." Presenting for Arm's involvement in the development, Gabriella Giuffrida, Arm's senior business manager for the flexible access program, said that doing the technology is "incredibly expensive" for a startup, so minimizing risk and providing access to the huge Arm ecosystem was important.

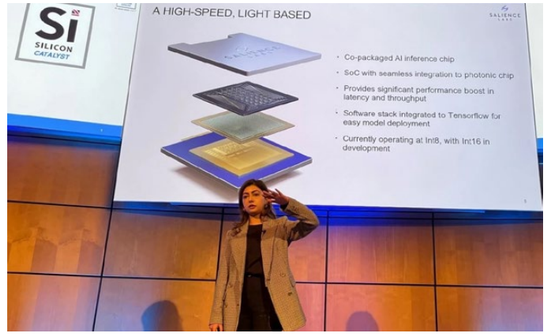
ARM'S FLEXIBLE ACCESS OVERVIEW

Arm's flexible access program starts free, and fees are introduced gradually as a startup goes through its funding stages.

Imec's ASIC design manager, Paul Ovington, talked about its role in helping Raspberry Pi get its MCU to market through its Imec.IC-Link unit. He said, "We help fabless semiconductor companies get their product to market." For Raspberry PI, they helped with the project management, packaging, test and qualification, tape-out support, and rapid production ramp.



Kashiff Siddiq, founder & CEO of Oxford RF Solutions



Vaysh Kewada, co-founder & CEO of Salience Labs

Jordan Mackellar, founder & CEO of Probe Test Solutions (PTSL) (Images: Nitin Dahad)

Joe Jones, Williams Advanced Engineering

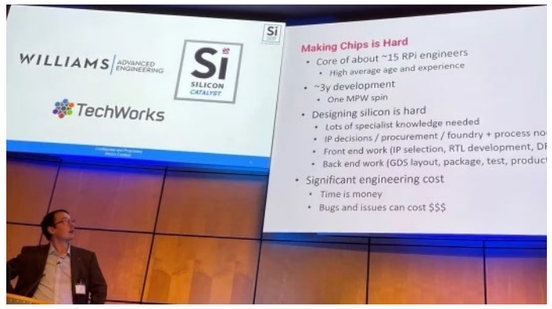
JAMES ADAMS HIGHLIGHTED THE KEY LEARNINGS FROM THEIR EXPERIENCE IN GETTING THE RP2040 OUT. HE SUMMARIZED IT AS FOLLOWS:

- Hiring in the right experience is important – both internal and external
- Leverage external experience, especially in navigating chip design complexities
- Leverage proven external IP, making sure not to reinvent the wheel but focus on your own unique selling point
- Build the virtual team that you need

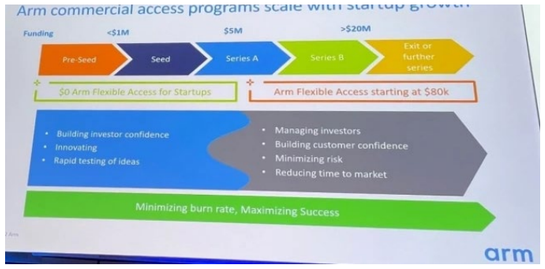
SERVING THE SILICON RENAISSANCE

Established first in 2015 in the U.S. by Rick Lazansky, Mike Noonen, Dan Armbrust, and Tarun Verma, Silicon Catalyst says it is the world's only incubator focused exclusively on accelerating semiconductor startups–including photonics, IP, MEMS, sensors, materials, and life science. Its model is providing support to startups through a network of in-kind and strategic partners to help dramatically reduce the cost and complexity of development. Silicon Catalyst supplies startups with a path to design tools, silicon devices, networking, access to funding, banking and marketing acumen to successfully launch and grow their companies' novel technology solutions.

As Richard Curtin, managing partner at Silicon Catalyst in the U.S., reminded me on a call this week, "There is a silicon renaissance", and he added that we should remind ourselves that semiconductors are the oxygen that allows software to breathe: a good reason for an incubator focused on silicon. The U.K. Silicon Catalyst chapter was launched last year with Sean Redmond as its managing partner.



James Adams Raspberry Pi



Arm's Flexible Access Program (Image: Nitin Dahad Data source: Arm presentation at Silicon Catalyst)

NITIN DAHAD

Nitin Dahad is a Editor-in-Chief of embedded.com, and a correspondent for EE Times, and EE Times Europe. Since starting his career in the electronics industry in 1985, he's had many different roles: from engineer to journalist, and from entrepreneur to startup mentor and government advisor. He was part of the startup team that launched 32-bit microprocessor company ARC International in the US in the late 1990s and took it public, and co-founder of The Chilli, which influenced much of the tech startup scene in the early 2000s. He's also worked with many of the big names - including National Semiconductor, GEC Plessey Semiconductors, Dialog Semiconductor and Marconi Instruments.

SILICON STARTUP SOLUTIONS

SiliconCatalyst.UK:
it all happens here®

Forming, Storming, Norming and Performing

A Silicon Catalyst event hosted by Williams Advanced Engineering

Silicon Catalyst, Williams Advanced Engineering and Techworks delivered the third in the series of our forming, storming, norming and then performing of UK semiconductor startup companies at the legendary Williams Formula 1 conference centre.

These events have been conceived to help new semiconductor founders learn from those experienced founders who have gone before. To share their learnings, both from the good things that happened and the bad. Deep tech semiconductor startups set themselves apart from other companies by the high level of technology risk they take on. These events help to amplify the benefits of the Silicon Catalyst ecosystem to reduce risk at each step of a semiconductor startups path to global success.

The opening address of the event was delivered by the CEO of Williams Advanced Engineering, Craig Wilson. He provided a fascinating insight into their world of high-performance automotive engineering and why semiconductors are at the bed rock of each improvement they make to accelerate the electrification of vehicles at ever reducing amounts of energy.

One of our most prominent UK Silicon Catalyst advisors, Dr Jalal Bagherli, presented his latest thinking on how to navigate our changing semiconductor world. As the hyperscalers increasingly underpin their technology stacks on semiconductor innovation and feed their need to own all the value they deliver to their customers, the drivers for semiconductor demand have radically changed. Jalal has witnessed this first hand as CEO of Dialog Semiconductors, where he expertly handled the opportunities and the threats that these new forces create.

Leaders from Williams Advanced Engineering team then took to the stage to share their road to electrification with deep dive insights into battery intelligence and the application of new innovations in power semiconductors. The need to drink from the fire hydrant of new semiconductor innovation shone through from Rob Millar, Tim Engstrom and Shaun Dawson all embracing the early adopter enthusiasm that used to be non-existent in the automotive industry.

Then it was all about the team from our Silicon Catalyst strategic partner Arm. Neil Parris, director for Partner success at Arm, along with one of UK's most successful new deep tech companies, Raspberry Pi and our In-Kind Partner Imec shared how the Arm Flexible Access program was instrumental in helping Raspberry Pi bring their latest world beating small compute platform to market through Imec's IC.link route to foundry.

After a well-received tea break and a tantalising glimpse of the history of the Williams Formula 1 racing cars we were back for what problem are you solving? It was the opportunity for two high class UK based semiconductor startups took to the stage. Firstly, Dr Kashiff Siddiq, the founder and CEO of Oxford RF explained how their 360-degree automotive radar is reducing the cost of detection in autonomous driving. Then our very own Portfolio Company CEO, Vaysh Kewada of Salience Labs projected the accelerated benefits of AI compute at the speed of light with their new hybrid approach to deliver on the insatiable demand from high performance engineering for more and more compute.

We concluded with an insight into how much money will semiconductor startups need? These talks covered three very diverse approaches to funding their paths to success. Jordan Mackellar, founder and CEO of Probe Test Solutions in the UK, shared his remarkable story of bootstrapping his business for more than a decade to a successful global scaling business. At which point he attracted nearly $40M of Private Equity backing to accelerate this global scaling to help take market leadership. The chair of our newest Silicon Catalyst UK Portfolio Company, QPT presented his learning from raising $1M of EIS Angel funding using an advanced subscription agreement shortly after being accepted into our accelerator. No funding story would be complete without our Venture Capital partners and Chris Wiles of the Foresight group did not disappoint. They have been one of the most active VC investors in UK semiconductor companies and clearly have the vision to help our sector flourish.

A huge thank you to all those that attended, contributed and most importantly Dr Jalal Bagherli, without whom this event would never have happened. Going shoulder to shoulder with Williams Advanced Engineering and our UK partner Techworks to put on this wonderful event to share with the leaders of the UK semiconductor industry has been an absolute pleasure.

REGIONAL
NEWSLETTER

Earth & Beyond Ventures - Bringing Israel 's Deeptech to Space

Earth & Beyond Ventures is a new Israeli venture capital fund which invests in groundbreaking early-stage Deep Tech & New Space startups. Earth & Beyond also operates an Israeli government sponsored incubator, where it guides towards success its young portfolio companies, which are striving to solve the largest challenges both here on Earth and deep in Space.

The fund is actively seeking Israel-based cutting-edge companies and research projects with potential Earth and Space applications operating across key deep tech sectors such as new space platforms, semiconductors, advanced sensors, optics & photonics, quantum computing, materials & nanotech, robotics and engineering, new energy, climate, agriculture and food technologies, and more.

Earth & Beyond Ventures is backed by leading multinationals and financial investors from Israel and abroad, including Corning, a US based material sciences, glass & optics, and ceramic company, Kyocera, a Japanese electronics conglomerate, Samtec, a US based electronic components company, Rhodium, a well-known Israeli investment firm, and Spacecom, an Israeli communications satellite operator, among others. The fund is also partnered with the Israeli government, having recently won a competitive tender process run by the Israeli Innovation Authority (IIA). The IIA provides significant match-funding on Earth & Beyond Ventures' investments, drastically increasing the investment capabilities of the fund.

Earth & Beyond Ventures' portfolio companies will receive an unparalleled experience including ongoing guidance, close ties with corporate partners, access to state-of-the-art lab facilities, and a wide network of multinational industry leaders and top investors.

In this context, Earth & Beyond Ventures is happy to collaborate with the Silicon Catalyst team in Israel, Danny Biran and Moshe Zalcberg. This collaboration involves sharing deal-flow, assisting in the screening and qualification of suitable ideas and possibly co-incubation leveraging the two organizations' respective strengths as relevant.

In addition to its investment activity, Earth & Beyond has established an ecosystem building business to work together with its investors and other key industry stakeholders to grow Israel

Earth & Beyond Ventures - bringing Israel Deeptech to Space!

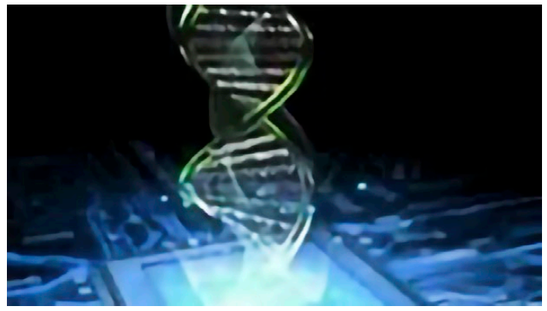
SILICON STARTUP SOLUTIONS

PORTFOLIO COMPANY NEWS
POLYN

POLYN Technology and Edge Impulse look to advance Tiny AI products

November 8, 2022 by Neil Tyler - newelectronics

POLYN Technology, a fabless semiconductor company that provides Neuromorphic Analogue Signal Processing (NASP) Tiny AI chips, and Edge Impulse, an embedded machine-learning (ML) development platform, are partnering to address ultra-low-power on-sensor solutions.



Targeting wearables, hearables, and the Industrial Internet of Things (IIoT), the collaboration aims to leverage the NASP platform to enable more customers to develop application-specific chips for one-dimensional signal processing at the sensor level and help expedite the adoption of ML at the edge.

"Resource-hungry edge devices present more and more complexity in sound processing, and this is an important challenge to address," said Aleksandr Timofeev, founder and CEO of POLYN. Additional challenges include power, accuracy, and novel capabilities. The Edge Impulse-POLYN collaboration will help vendors resolve these issues in next-generation products."

POLYN's NASP development framework provides fast conversion of trained neural networks from any well-known ML library into neuromorphic analogue chips. Neural-Net-To-Chip automation tools provide a fully functional simulation of the resulting math model, converting it into chip production files. These tools dramatically reduce product time to market, CAPEX, and redesign OPEX.

POLYN's business model has been designed to provide customer support throughout the entire product development cycle, including neural network selection, training, optimisation, and testing on the software simulation. The size and structure of the neural network is always optimised to the customer's task, delivering a cost-effective development of tailored solutions that perform deep learning computations on mass-market devices.

Edge Impulse's machine learning software supports the development of smarter edge products, providing powerful automation and low-code capabilities to make it easier to create valuable datasets and develop advanced ML algorithms.

The company's technology enables developers to bring more ML products to market faster, and helps teams rapidly develop industry-specific solutions in weeks instead of years.

"We're very excited to work with POLYN to help nurture brand-new solutions using our respective technologies," said Zach Shelby, CEO and co-founder of Edge Impulse. "The combination of their IP and our platform provides opportunities for users to overcome development challenges while finding valuable new applications for their data."

POLYN and Edge Impulse are focusing initially on hearables and will look to develop novel designs for hearing aids, hearing assistance products, earbuds, and other miniature devices.

PORTFOLIO COMPANY NEWS
POLYN

CEO Interview: Aleksandr Timofeev

October 21, 2022 by Daniel Nenni - SemiWiki.com

Aleksandr Timofeev is CEO and Founder of POLYN Technology, an innovative provider of ultra-low-power high-performance NASP (Neuromorphic Analog Signal Processing) technology. Alexander is a serial entrepreneur with more than 20 years in the high-tech industry. Prior to POLYN, he founded iGlass Technology, a company that developed novel electrochromic smart glass technology. He built the core team, general technology, and product concept and successfully sold the company at the end of 2020 to a strategic investor. Aleksandr is also founder and managing partner at FPI VC team, an early-stage venture investment management company. The fund focuses on early-stage innovative companies, developing clear product concepts and strategies and working with venture firms and partners for subsequent funding rounds.

While looking at the landscape of new startups in the AI/ML industry I found POLYN. The company differs from others in its business model as well as its concept and technology approach.

POLYN is a fabless semiconductor company selling ready-to-use Analog Neuromorphic chips as Application Specific Standard Products, targeting specific technological challenges in huge and fast-growing markets, particularly wearables, connected health, and Industry 4.0. Founded in 2019, it is registered in the UK with HQ in Israel.

According to its website, POLYN offers two products, and one more is under development. Recently it was announced that POLYN was accepted into the Silicon Catalyst incubator family.

We talked with Aleksandr Timofeev, CEO and founder, to explain the technology and what he is up to now. We asked Aleksandr's opinion on today's neuromorphic computing, what is special about POLYN, and how far we are from a real Tiny AI solution working on the sensor level. Here's the interview:

Q: FIRST, CONGRATULATIONS ON JOINING THE SILICON CATALYST INCUBATOR COULD YOU SAY FEW WORDS ABOUT WHAT IS IN IT FOR POLYN?

AT: POLYN's objective as a fabless semiconductor company focusing on ready-to-use analog neuromorphic chips is to collaborate with leading semiconductor vendors, industry partners, and entrepreneurs. Our mission is to introduce novel analog neuromorphic solutions for wearables, hearables, and IIoT on-sensor pre-processing with highly efficient energy per inference ratio. By being part of the Silicon Catalyst community and its huge portfolio of partners, we expect to accelerate our plans to improve cost, time to market, and the reach of our unique technology.

Q: I SEE YOUR COMPANY DECIDED TO GO A DIFFERENT WAY WITH CONSTRUCTING A CHIP FROM A NEURAL NETWORK, UNLIKE MANY OTHERS WHO ARE DEVELOPING GENERAL PURPOSE PROCESSORS TO APPLY A NEURAL NETWORK THERE?

AT: Yes, we decided that for a neuromorphic based product it is more efficient to synthesize a chip from a neural network model, not like in the digital domain where you have fixed, general purpose PU instruction sets, and different software applications using them. When you start training a neural network (NN), you don't know what final size you will get. If you have a fixed neuromorphic core, for some NNs it will be too small, and for others too big.

Q: OK, INTERESTING, BUT THAT MEANS YOU NEED TO GENERATE A LOT OF CHIPSETS AND THAT WOULD BE BOTH TIME AND COST CONSUMING. HOW YOU ARE DEALING WITH THAT CHALLENGE?

AT: We are focused on the ASSP model. Our chip is related to sensor or signal type, but not a sensor model. For example, our Voice Extraction NASP chip works with any type of analog or digital mems microphone and other signal sources. And we will generate a new NASP core only for a new sensor or signal type. As you understand, it covers millions of products. In case some new product moves to a different physical device, we can upgrade the chip easily, thanks to our fully automated process. So, to summarize, first NASP is application-specific and not product-specific, so the volumes are huge. Second, moving from application to application is easy with the POLYN automation tools. By the way, our tools were the first technological achievement at the beginning of the company, and they remain a unique EDA instrument for neural network conversion.

SILICON STARTUP SOLUTIONS

Q: VERY IMPRESSIVE, BUT I HAVE ANOTHER QUESTION: YOUR CRITICS COULD SAY THAT IMPLEMENTING EVEN THE INFERENCE NEURAL NETWORK MODELS REQUIRES CHANGES, AND AS A RESULT YOUR NEURAL NETWORK WILL NEED TUNING FROM TIME TO TIME. IF YOUR TECHNOLOGY IS IMPLEMENTED IN A FIXED RESISTOR LAYER, HOW DO YOU SUPPORT NEURAL NETWORK CHANGES AND UPDATES?

AT: First, we use the fundamental property of a neural network: when you train a deep neural network, after a few hundred training cycles a major part of the layers will become frozen. So typically, about 90% of layers are not changing anymore, and are not involved in the following updates. Only a few last layers require an update if you need to change the classification. In such case we use a hybrid solution: the 90% layers are converted into a high performance NASP core and the last 10% remain in the flexible digital domain. But it is important to remember that our solution is focused on sensor level applications. We are not simulating brain functions, where constant learning (or re-training) is critical. In many sensor-level applications the pre-processing task is fixed and doesn't require any update.

Q: LET'S DISCUSS THE ANALOG PART. I MEAN, WHO WOULD IMAGINE WE COME BACK TO ANALOG AFTER GETTING DIGITAL WITH MILLIONS OF TRANSISTORS ON A CHIP AND TALKING TODAY ABOUT 2NM PROCESS? WHY DO YOU THINK ANALOG IS A RIGHT OPTION FOR COMPLEX MATH MODELS AS NEURAL NETWORKS?

AT: First of all, we are talking about neuromorphic analog, which is not like old style analog computers. We represent a trained neural network using analog neurons. The fundamental property of this structure is true parallel data processing.

Any digital system has step-by-step execution. But the human brain, one of the most power-efficient computation devices, uses parallel data processing. It is important to note that POLYN is mimicking not the central brain but peripheral systems. We are at the sensor level where the main idea is pre-processing, removing noise, extracting data, and here the analog is irreplaceable. Digital can go down in the process, but for Joule per Inference ratio, analog will win.

Q: ANY MORE ARGUMENTS FOR ANALOG? FOR EXAMPLE, HOW DO YOU RESOLVE THE ANALOG IMPLEMENTATION NOISE ISSUE? WHAT IS THE PRODUCT DEVIATION ON THE MATH MODEL?

AT: The answer again lies in the term "neuromorphic," as neural networks are implemented in a neuromorphic analog circuit. The point is that resilience to errors is a fundamental property of neural networks, and training increases the resilience.

Circuit non-idealities can be divided into two groups: random and systematic errors.

Systematic errors occur because a typical circuit implementation only approximates an ideal signal processing operation to a limited extent. Such errors are caused, for instance, by the non-linear operating characteristics of devices or by finite gain of an analog amplifier.

Stochastic errors may happen during the fabrication of integrated circuits and result in a random variation of the properties of the fabricated on-chip elements. These errors, however, can be modelled and addressed during development. For example, the mismatch between neighboring elements is usually much smaller than the variation of parameters' absolute values. Therefore, differential architectures could significantly improve precision.

For an analog circuit design, it is important that such errors do not accumulate. For this, the neural networks are trained using special technology for error compensation

Q: INTERESTING. COULD YOU TELL US ABOUT THE BIRTH OF POLYN AND THE IDEA OF YOUR TECHNOLOGY?

AT: I met Dmitry Godovsky, our Chief Scientist, at the end of 2018. Dmitry worked eight years previously on a new math model of converting a digital neural net to a new implementation. After few months of discussion, we understood that this new model can be represented as a neuromorphic analog circuit. So, in April 2019 we launched POLYN Technology. Since then, we have constantly invested in know-how and innovation. Today we have 25 patents for the technology and products.

Q: NATURALLY, THIS RAISES THE QUESTION: WHAT ABOUT FABS? COULD THEY RUN THE FABRICATION IMMEDIATELY, OR DO THEY NEED TO ADAPT THEIR PROCESSES? BY THE WAY, THE SAME QUESTION APPLIES FOR THE PDK AND EDA TOOLS YOU ARE USING FOR THE CHIP DEVELOPMENT.

AT: Our strong advantage is that we are using any standard process in 40-65 nm range and can align our product libraries to any standard PDK. Our NASP compiler and physical design

PORTFOLIO COMPANY NEWS
QPT LIMITED

QPT Gains Admission to the Silicon Catalyst Incubator

Clean-tech specialist gains strategic endorsement in its mission to save energy

Cambridge, UK, October 12, 2022 - SiliconCatalyst.UK is pleased to announce that QPT Limited, the clean-tech company focusing on electrical efficiency, has been accepted into the Silicon Catalyst Incubator programme. QPT will have direct access to the products and services of the Silicon Catalyst comprehensive ecosystem of In-Kind Partners and a wealth of industry expertise through the advisor and investor network.

QPT is a semiconductor startup company with a vision to help the world save energy through the development of unique IP that can revolutionize power electronics systems, radically improving efficiency and performance. The company has developed unique new approaches to controlling transistors with very high-speed GaN transistor drivers with picosecond timing precision (low jitter isolation) and digital control loops (based on a novel ADC architecture) combined with converter topologies drawing on RF techniques and understanding of power transistor device physics. The resulting precision timing and high-speed operation provides ultra-low loss switching for motor drives, reducing losses by up to 80% which results in less heat, less cooling, less weight and greater capacity.

Silicon Catalyst has built an ecosystem of unrivalled support for semiconductor start-ups, granting privileged access to EDA design tools, silicon foundry runs and intellectual property. The incubator provides networking, access to finance and expert business acumen to successfully launch and to drive growth. This announcement highlights the regional importance and focus from Silicon Catalyst for innovative semiconductor enterprises based in the UK.

Commenting on the news, QPT Founder and CEO Rob Gwynne said, “Our acceptance into the Silicon Catalyst programme is a huge endorsement for our mission to save energy and underlines the importance of our products in the power electronics industry. Electric Motor Driven Systems (EMDS) consume 45% of the world’s energy, and yet their efficiency at typical operating speeds can be as low as 50%. Our new qGaNDrive™ module has a completely new and patented approach for driving GaN transistors for electric motors driven systems. This fully EMC-screened, turn-key, power module improves power efficiency across the range of operating speeds.”

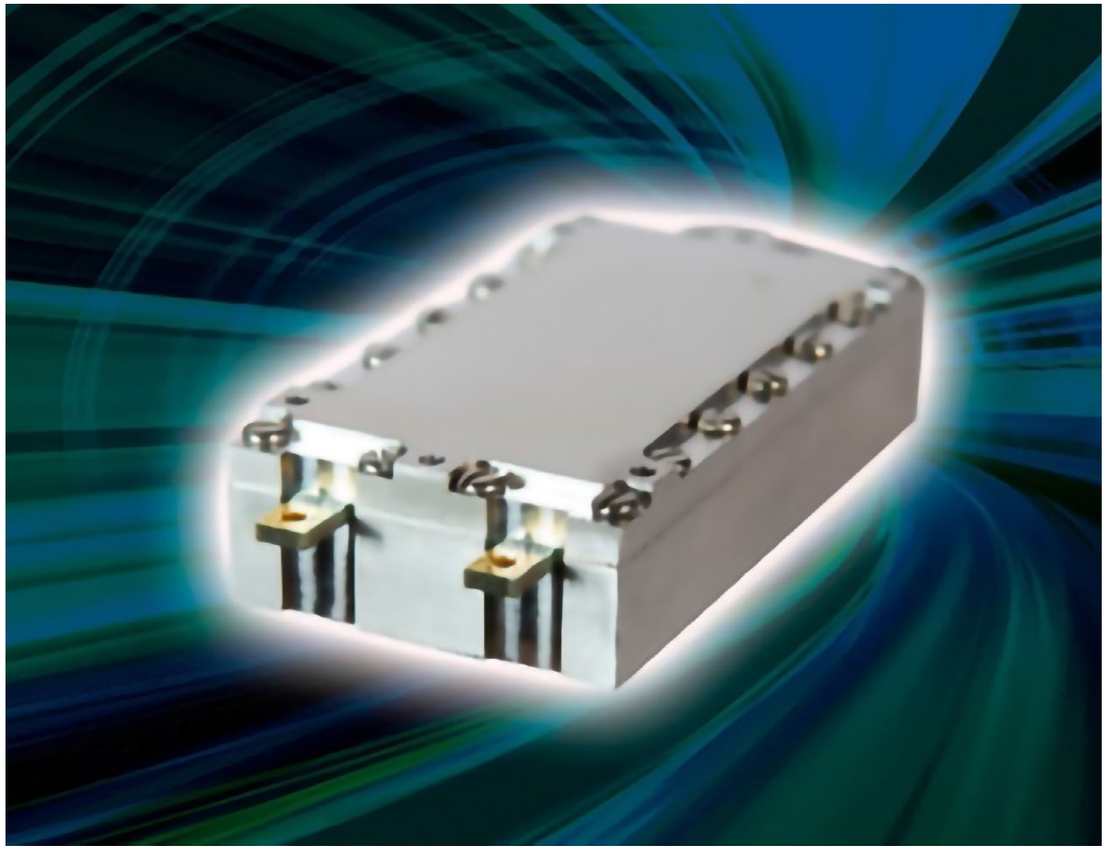
GaN transistors have always promised the best performance and efficiency, but current design approaches have failed to achieve these benefits because they cannot be driven at the high frequencies needed to deliver them. The patented QPT technology unlocks the potential of GaN to provide significant power savings by enabling GaN transistors to be driven at these high switching speeds. Reducing the energy use of this huge sector could have a real impact on helping reduce climate change.

Sean Redmond, Silicon Catalyst UK Managing Partner, went on to add “QPT has progressed through each stage of our rigorous screening process, and we’re delighted to welcome Rob and the team into our portfolio. We’re really keen to leverage our experience, network and partners to accelerate QPT in its business growth to become a premier climate tech company.”

ABOUT QPT LIMITED TECHNOLOGY

Established in Cambridge in 2020 as an independent power electronics company, QPT™ specialises in the delivery of high-performance, efficient, and cost-effective solutions to solve the challenges of designing with Gallium Nitride transistors. QPT™ technology unlocks the potential of GaN to provide huge power savings across a wide range of electrical devices. In particular, motors that currently account for 45% of the global power budget. Its first innovative power module increases power efficiency from as low as 50% to up to 99.5% to reduce power losses in motor drives. Key application areas that account for a significant share of global power consumption include heat pumps and HVAC (heating, ventilation, and air-conditioning) systems. Please visit www.q-p-t.com, or contact on info@q-p-t.com for further information. qGaNDrive and QPT are trademarks of QPT Limited.

SILICON STARTUP SOLUTIONS



QPT’s new qGaNDrive power module is a drop-in replacement for existing modules

“Our acceptance into the Silicon Catalyst programme is a huge endorsement for our mission to save energy and underlines the importance of our products in the power electronics industry.”

ROB GWYNNE – QPT FOUNDER AND CEO

PORTFOLIO COMPANY NEWS
POLYN TECHNOLOGY

Silicon Catalyst Announces POLYN Technology as Newest Company Admitted to Semiconductor Incubator

Delivering Innovative Neuromorphic Analog Signal Processing

Silicon Valley, California, and Caesarea, Israel - September 29, 2022 - Silicon Catalyst, the world's only incubator focused exclusively on accelerating semiconductor solutions, announces the admission of POLYN Technology into the semiconductor industry's highly acclaimed program. POLYN Technology is an innovative provider of ultra-low-power-performance NASP (Neuromorphic Analog Signal Processing) solutions and a producer of unique Tiny AI chips and their associated IP.

POLYN's NASP-based Tiny AI inference solutions are ideally suited for always-on smart devices performing sensor data pre-processing in a wide variety of Edge AI applications, including human health monitoring, hearing assistance, and machine condition monitoring.

"POLYN's mission is to collaborate with leading semiconductor vendors, industry partners and entrepreneurs to introduce next-generation sensor data pre-processing solutions for wearables, hearables, and Industrial IoT predictive maintenance. Our team of deep learning and chip design experts with experience in such industry giants as Cadence, Intel, LG, Marvell, Sony, and Tower Semiconductor, successfully released the first NASP Test Chip, demonstrating proof of the technology's brain-mimicking architecture and tools. It is the first Tiny AI true analog design to be used next to sensors," stated Aleksandr Timofeev, founder and CEO of POLYN. "By being part of the Silicon Catalyst Incubator and its broad portfolio of partners, we'll accelerate our plans to improve cost, time to market and reach of our unique technology".

Silicon Catalyst provides critical support to semiconductor hardware startups as they move from idea through prototype to initial product. Since its founding in 2015, Silicon Catalyst has reviewed over 700 early-stage companies and has admitted 85 startups into the incubator.

WHY CHOOSING **NASP**

NASP Chip Offloads AI Processing
of Sensor Data from MCU

"Silicon Catalyst's mission is to assist innovative semiconductor startups in their journey to success", added Moshe Zalcberg, Silicon Catalyst's General Partner in Israel. "POLYN offers a disruptive technology that has the potential to make a major impact in several key markets, and we're happy to partner with Aleksandr and his team in making this a reality".

ABOUT POLYN TECHNOLOGY

POLYN Technology is a fabless semiconductor company, supplying ultra-low-power, high-performance Neuromorphic Analog Signal Processing (NASP) technology, IP and Tiny AI chips based on NASP. POLYN's Neural-Net-To-Chip automation tools support the fast and cost-effective development of tailored Tiny AI solutions, which perform AI computations on-device. The technology and products enable a wide range of edge AI applications with power consumption, accuracy, size, and cloud connectivity constraints, like wearables, Industry 4.0, Connected Health 4.0, Smart Home and more. POLYN Technology was founded in 2019. The company is registered in London and headquartered in Israel. Learn more at www.polyn.ai

PORTFOLIO COMPANY NEWS
EXOKERYX

Silicon Catalyst Announces Exokeryx as the Newest Portfolio Company Admitted to the Incubator

Early-stage company developing diagnostic solutions to revolutionize early detection of cancer and other diseases

San Diego, CA and Silicon Valley, CA, November 16, 2022 - Silicon Catalyst, the world's only incubator focused exclusively on accelerating semiconductor solutions, is pleased to announce that EXOKERYX has been accepted into the Silicon Catalyst Incubator program. With their admission into the Incubator, EXOKERYX will have direct access to the products and services of the Silicon Catalyst comprehensive ecosystem of In-Kind Partners and a wealth of industry expertise through the advisor and investor network.

EXOKERYX is revolutionizing tools for early disease detection and diagnosis by combining the power of solid-state electronics with exosome based biomarker discovery. Current diagnostic methods often catch cancer too late and result in therapy pathways that are as harmful as the disease itself. By combining principles from the semiconductor industry with breakthrough biotechnology EXOKERYX is seeking to transform how cancer and other diseases are detected and treated.

Exosomes are crucial to cellular communication within our bodies and hold one of the keys to early cancer and disease detection. Armed with this knowledge, EXOKERYX is developing a bio-chip platform for analyzing biological samples. This interdisciplinary approach will use the, all-digital EXOKERYX, lab-on-a-chip device to perform a liquid biopsy that isolates, quantifies and analyzes exosomes. The enhanced sample will subsequently be used for identifying biomarkers that direct the detection and treatment of cancer and other diseases. The company leverages its extensive experience in biological analysis and semiconductor technologies to create the converged approach which will provide fast, cost-effective detection that can be deployed on a global basis.

EXOKERYX CEO, Richard Young states: "We see a future where we can interrupt and stop disease progression in asymptomatic patients by finding it when they go to their annual physical. That vision fuels every member of our team. We have a clear path to provide an early-detection platform for a variety of cancers," said Richard Young. "We see Silicon Catalyst as a valuable partner that can help accelerate the development time and position the company for growth in the next two years."

EXOKERYX joined Silicon Catalyst to take advantage of the extensive array of resources provided by the Silicon Catalyst ecosystem to assist with the development, commercialization, and market traction. With a singular focus on semiconductor and sensor technologies, Silicon Catalyst has dedicated itself to accelerating emerging hardware technologies that require microfabrication.

"We have seen an influx of applications from startups developing novel bio and life science technologies. The mission of EXOKERYX to dramatically improve the techniques for early-stage cancer and serious disease detection is one that Silicon Catalyst is pleased to support with the full force of our resources," said Pete Rodriguez, CEO of Silicon Catalyst. "The impact of these capabilities offers the prospect to improve the lives of everyone on the planet, and we applaud the urgency the EXOKERYX team has demonstrated to commercialize the products for deployment in the battle against cancer."

ABOUT EXOKERYX

EXOKERYX is based in San Diego, California, considered one of the world's top biotech centers. The founding team is multidisciplinary and broadly experienced in research, development, volume manufacturing, and compliance. Richard Young, CEO of EXOKERYX, has an extensive background in manufacturing, operations and finance and has worked in executive leadership for over 20 years. Bryan Rice Ph.D., CTO of EXOKERYX, has a broad semiconductor background, having started his career at Intel and then moved to Sematech, Global Foundries and several biotech companies. Amber Murray, Ph.D., leads the bio-assay product development and brings extensive experience in biotech product development at Exact Sciences and other biotech companies doing liquid biopsy and bio-analysis products. More information is available at: https://exokeryx.com/

PORTFOLIO COMPANY NEWS
IN-KIND PARTNER PROFILE

Silicon Catalyst Expands In-Kind Partner Ecosystem with 3 UK-based Companies

Alter Technology, Codasip & Crypto Quantique join semiconductor incubator

Silicon Valley, California and London, United Kingdom, November 28, 2022 - Silicon Catalyst, the world's only incubator focused exclusively on accelerating semiconductor solutions today announced three new In-Kind Partner (IKP) companies: Alter Technology TUV NORD UK, Codasip and Crypto Quantique. These IKPs will provide support to the companies in the Silicon Catalyst Incubator, further expanding the comprehensive ecosystem that enables early-stage companies to tap into the products and services available to enhance the growth of their companies.

THE NEW IKP ORGANIZATIONS INCLUDE:

Alter Technology UK, a leading supplier of fast turnaround prototype assembly and volume packaging of Microelectronics and Photonics assembly for semiconductor devices

Codasip, the leader in customizable RISC-V processor IP

Crypto Quantique, a supplier of quantum-driven hardware root-of-trust design IP

Silicon Catalyst has built an ecosystem of unrivalled support for semiconductor start-ups, granting privileged access to EDA design tools, silicon foundry runs and intellectual property. The incubator provides networking, path to funding and expert business acumen to successfully launch and drive growth. This announcement further highlights the regional importance and focus from Silicon Catalyst for innovative In-Kind Partners to enable business growth for the Portfolio Companies in the incubator.

SEAN REDMOND, SILICON CATALYST UK

"We are relentlessly expanding our ecosystem to serve the best semiconductor start-ups in the industry. Our Portfolio Companies do not need to compromise on any choice they need to make by getting access to exactly what is required to be successful as globally scaling semiconductor companies. We are delighted to welcome Alter Technology, Codasip and Crypto Quantique to our In-Kind Partner program, enhancing our ability to provide flexible and scalable device packaging, application-specific RISC-V processors and root-of-trust design IP solutions to support the product needs of the innovative companies in our Incubator."

Alter Technology TÜV Nord UK Ltd has started volume production of plastic encapsulated QFN chip packages in the UK. Most of the semiconductor packaging is currently taking place in sizeable out-sourced assembly and test (OSAT) production lines in Asia, so the Alter plant in Livingston, Scotland, offers a significant capability in the UK. Traditionally UK semiconductor packaging has been centred on low volumes using ceramic and metal packages with batch sizes restricted to 100s of devices packaged in a sequential pattern. The change to this lower-cost and high-volume compatible plastic package technology signifies a 90% decrease in cost and facilitates several thousands to tens of thousands of devices per batch. Alter UK also offer advanced packaging processes and solutions for custom photonics components.

Stephen Duffy, Chief Executive Officer of Alter Technology TÜV Nord UK Ltd said, "Silicon Catalyst's Portfolio Companies are all on a trajectory to ship large volume semiconductor devices to their global customer base. Being able to work closely with them through their prototype packaging needs all the way to their low-cost large volume packaging final production shipments is a great opportunity for us to work with those startups that we are confident will succeed".

Codasip is the leader in customizable RISC-V processor IP. With their Codasip Studio customization tools, chip designers can create highly differentiated application-specific RISC-V processor design IP.

Ron Black, CEO, Codasip, commented, "Many semiconductor startups are now struggling to achieve performance gains from scaling semiconductors to smaller nodes. Early adopters of application-specific IP design are seeing the benefits of tailoring their processors to their target markets. Our RISC-V processor design IP combined with the customization capabilities of Codasip Studio enables them to make significant performance gains."

Crypto Quantique is an IoT security pioneer that has combined cryptography and quantum physics to develop security products that drive end-to-end security and unlock scalability for IoT networks.

Dr. Shahram Mossayebi, CEO and Co-Founder of Crypto Quantique said, "We are delighted to join Silicon Catalyst as part of the In-Kind Partner program, aiming to bring enhanced IoT device security for startups and scale-ups. Our QDID design IP, which has been independently verified as robust against all known cyberattack mechanisms, measures quantum effects occurring in the fabric of silicon wafers to produce unique, unforgeable identities and cryptographic keys on-demand inside chip designs. The identities and keys create roots-of-trust for the chips used in IoT devices and edge nodes. QDID is a second-generation physical unclonable function (PUF) that eliminates key injection and the requirement to store keys in device memories."

PORTFOLIO COMPANY NEWS
KURA TECHNOLOGIES

KURA

CEO Interview: Kelly Peng

April 1, 2022 by Daniel Nenni - SemiWiki.com

This interview is with Kelly Peng, Co-founder, and CEO of Kura Technologies. Kura Gallium, Kura's first product, was named Best of CES 2022 and received a 2022 CES Innovation Award as well. Kelly is an inventor, engineer and entrepreneur that leads a team of dedicated innovators that are redefining the term "Augmented Reality". She was a recipient of the prestigious Forbes "30 Under 30" in 2019 for her work in developing the most advanced augmented reality glasses that will start sampling in 2022. Based in Silicon Valley, Kura Technologies is eclipsing the competition in areas of field of view, resolution, brightness, transparency, depth of field, sizes, and other critical metrics.

WEB3 AND IN PARTICULAR AUGMENTED REALITY IS A HOT TOPIC CURRENTLY, HELP OUR READERS UNDERSTAND WHAT DIFFERENTIATES KURA FROM THE MANY OTHER EARLY-STAGE COMPANIES IN THIS MARKET.

As you have indicated, the interest in Virtual Reality and Augmented reality is currently expanding in all directions. The fact is that we are currently experiencing a rapid change in the way AR and VR will be deployed in the very near future. These changes will open up new markets that were inconceivable a few years ago and will allow us to interact with information in the world around us in practical and interesting ways. The emerging applications will enable new activities like medical diagnosis and treatments, training, 3D design visualization, industrial inspection, and face-to-face virtual communications all through a pair of glasses.

To facilitate this, Kura has focused our technology development to create a visualization system that is as natural as wearing glasses, and allows the wearer to experience the enhanced content necessary to optimize the desired reality. The Kura Gallium is the first pair of AR glasses to offer a 150-degree full frame field of view, 95% transparency, 8K resolution, unlimited range of depth, and many other features that provide the seamless view of the natural and augmented surroundings often referred to as the "Metaverse".

WHAT IS THE STATUS OF THE GLASSES THAT WERE DEMONSTRATED AT CES IN JANUARY?

We showed demos with the world's biggest field of view in AR, high transparency, and high brightness; newly assembled eyepieces for our upcoming dev kits, and software applications including3D model viewers and telepresence and remote collaboration tools running on our headset with 9-degree of-freedom head-tracking and gesture input. The team is focused on a couple of major developments for the hardware and telepresence platform side of Gallium. One of the larger projects is the development of the ASIC that creates the backbone of the system electronics. Custom ASICs and silicon were taped out last Fall at some of the world's biggest production foundries and we are pleased to announce that the silicon has already come back from the fab and has also been packaged. We have been testing and running characterization recently and the results look great. The tape-out is a big success!

CAN YOU PROVIDE SOME MORE DETAILS ABOUT THE ASIC?

Yes, the internal code name for the chip is "Mill's Creek". The chip incorporates the control and driver circuits for the micro-LED displays, as the world's fastest micro-LED display driver ASIC and core enabler for our 8K resolution. This is one of the most critical components in the systems because it provides more than 100x resolution expansion, on-the-fly pixel repair, high dynamic range and full-color images.

The Augmented Reality user experience is dependent on high-quality display capabilities. The Gallium glasses use fully customized micro-LED displays to create the brightness and image sharpness that people expect. However, the micro-LED technology is not optimized unless the display driver and our optical architecture are optimized specifically for the application. The "Mill's Creek" ASIC is fully customized specifically for the Kura Micro-LED display hardware with a completely unique architecture, which is unlike practically all of the other headsets that use off-the-shelf components for the display driver. This successful tape-out is a big milestone for us toward pushing Gallium to production.

SILICON STARTUP SOLUTIONS

STARTUP COMPANIES ARE ALL ABOUT THE TEAM OF ENGINEERS AND INNOVATORS THAT ARE DRIVING THE DEVELOPMENT. CAN YOU GIVE US A LITTLE MORE INSIGHT INTO THE TEAM?

Kura is currently made up of over 35 people that are all contributing to the product development. We have been very fortunate to pull together a great mix of talent. More than half of Kura's founding and leadership are from MIT, and 3 of our lead engineers have together of 400+ patents. Kura's in-house ASIC design team leader is Mark Flowers, Kura's Director of Technology, who was previously the founding CTO of Leapfrog (IPOed, and valued $1B+). He has over 30 years of leadership experience designing and delivering custom mixed-signal ASICs. In the past, he was responsible for the shipment of tens of millions of customized chips as well as integrated consumer and enterprise platforms and products. In an earlier startup, Mark was the co-inventor of DSL, with over 800 million installed lines. That company was acquired by Texas Instruments. He graduated from MIT with a Master's and Bachelor's in electrical engineering with a specialty in IC design and computer science.

We are also fortunate to have a strong operations organization. That team is led by Gregory Gallinat, our COO, and Chuck Alger, Director of Supply Chain and Manufacturing. A core focus of the Ops team is defining and facilitating the worldwide supply chain and business practices to support Kura's product launch and growth trajectory. Chuck has more than 20+ years of experience with Intel, Microsoft, and CP Display. This includes multiple manufacturing site launches for products like Hololens and Surface. He also has extensive expertise in semiconductor quality and reliability coming from his time at Intel. Chuck also worked as Director of Supply Chain at Compound Photonics (just acquired by Snap), a company building ASICs for driving micro-displays like micro-LED and LCoS.

WHAT'S THE DEMAND AND UPCOMING ADOPTION OF KURA GALLIUM?

We are a platform company poised to reshape the landscape of AR. The interest in Kura Gallium has been fantastic in the last year. The CES awards and the exposure we received through various other venues has opened up the path to adopt the platform into a broad range of applications. The various venues where we have been invited to speak at such conferences as SPIE, has exposed our thought leadership to this market. Kura currently has orders from over 350 companies, 100% of which are in-bound, and among those, over 50 companies that are in the Fortune 500, with total order requests from paid Fortune 500 companies totaling more than 100K units, and as these companies recognize the superiority of our performance and plan to use our product and platform in such areas as remote collaboration, telepresence, virtual showrooms, training, entertainment, tele-medicine, etc..

Many of these clients had also become investors in Kura. We also have several active projects with government agencies that see Augmented Reality as a critical technology for training, visualization, and remote collaboration and assistance. As you can see, the need for AR in various enterprise applications is very high now and we see many of these adopting our product quickly, as many clients and repeatedly express to us they really want to have the headset deployed as soon as possible. The CEO of Tokens .com, a publicly traded company that invests in Web 3 assets recently said in an interview on CNBC that "within the next 24 months all major companies will have a presence in the Metaverse like they have a website."

YOUR INITIAL FOCUS SEEMS TO BE ON THE ENTERPRISE AND B2B2C SIDE. WHEN WILL CONSUMERS BE BUYING KURA GALLIUM?

As with most emerging technologies, the early adopters start with the enterprise market. The enormous benefit of having real-time information augmenting that forward-looking view of users can be realized quickly in many industries. We are launching our hardware + software platform (global holographic telepresence platform, computer vision/AI SDK, and AR data platform), and many of our clients are industry leaders or some of the biggest companies in the world in automotive, training, design, telecommunication, entertainment, etc.

AR is really an industry in that demand had been waiting long for a product that users can use with acceptable vision quality together with a good form factor, Kura's product and platform are serving the biggest demand in the industry and also largely expand the number of use models. Not to mention, Kura's performance combined with the comforts of our first product over-compete all the "consumer-targeted" AR glasses and solutions today already. The consumer demand is there and will grow rapidly following the enterprise adoption, with a rich set of applications like the App Store. We have already designed many of the core technologies for our future generations of products that will be launched for both consumers and enterprises with improved performance and even more compact with a deeper level of silicon integration.

PORTFOLIO COMPANY NEWS
KURA

Kura Technologies Partners with TSMC to Build the Future of the Metaverse

June 14, 2022 by Globe Newswire

Kura Technologies, an award-winning developer of the best-in-class augmented reality (AR) smart glasses and platform, today announced a manufacturing collaboration with TSMC to build its initial custom micro-LED display chipset (customized integrated circuits/silicon), which is a key enabler for many of Kura's ultra-high performance and platform features.

Kura's custom mixed-signal display driver integrated circuits (DDIC) and other supporting devices, which enable industry-leading performance, have already been successfully taped out on a standard, high-volume CMOS node at TSMC. This DDIC, which represents both the smallest process node ever used on a micro-display driver as well as the world's fastest micro-LED driver, is a key element of Kura's award-winning first product, Kura Gallium smart glasses.

"We're pleased to work with TSMC, a collaborator from the early days of Kura, to successfully tape out our mixed-signal micro-LED display driver, which is the world's fastest and a key enabler for our 8K resolution, as well as other platform features and ultra-high performances," said Kura's Founder, CEO and CTO Kelly Peng. "More importantly, these specs solve some of the biggest performance bottlenecks in AR adoption—from field-of-view to text readability for use cases from training to telepresence. We're grateful for the support provided by TSMC to advance our mission to deliver the best performing AR glasses at scale and help make the Metaverse a reality."

Kura Gallium smart glasses have the highest performance in the industry, with 8K resolution using full-color, ultra-high brightness, and production-ready micro-LED displays—an industry first no other company has achieved. Kura's DDIC enables on-the-fly defect and nonuniformity correction, allowing the company's displays to tolerate 10,000 times the defect rate and four times the brightness variation of any other AR devices or micro-LED display use cases. This puts Kura years ahead in production, and drastically improves their yields, compared to any other players, letting them go to market with currently-available, economically-manufacturable micro-LED displays 5+ years ahead of the rest of the industry.

In addition, Kura has also received its customized micro-LED display in wafers in multiple colors, and is working with key partners and manufacturers to scale for production.

AR represents a $1.3 trillion market opportunity with some of the biggest applications ranging from telepresence, design visualization, and remote collaboration to training, entertainment, and more.

Kura's AR glasses are the first to offer a 150-degree full-frame field-of-view (9x of existing AR devices), 95% transparency (4x), 8K resolution, and unlimited range of depth, among other features that provide seamless views of natural and augmented surroundings. Gallium's high transparency allows users to safely wear the glasses in various environments while maintaining natural eye contact, and simultaneously operating equipment, control panels, and computers.

And Gallium's high angular resolution is the highest among all AR glasses at 60+ pixels per degree, which is crucial for viewing fine details and reading text. Equally important, Kura's optical design and eyepiece do not leak light to the front, and others cannot view what the user is seeing on the screen, ensuring privacy, safety, and comfort.

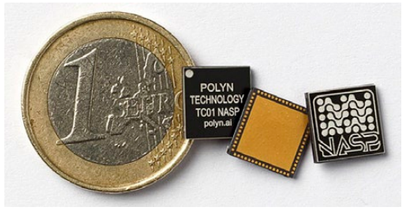
"Kura's vivid, immersive and clear images enable broad use cases for product design, training, production and visualization. Enterprises in automotive and other manufacturing industries will benefit greatly from these new possibilities," said Ye Wang, Investment Principal at SAIC Capital, the corporate venture arm of one of the world's largest car manufacturers, and one of Kura's early investors.

SILICON STARTUP SOLUTIONS

PORTFOLIO COMPANY NEWS
POLYN

POLYN has developed an Analog Neural Network Chip

June 21, 2022 - TechTime



The new concept is based on a mathematical discovery that allows for the representation of digital neural networks using operational amplifiers and resistors - to achieve high speed and lower power consumption

Polyn Technology plans to introduce a novel Neuromorphic processor chip, based on analog electrical circuitry, unlike the standard digital neural networks. Lately, GlobalFoundries has completed the production of the first trial batch in a 55nm CMOS process. Alexander Timofeev, CEO and co-founder of Polyn Technology told Techtime that the chip's commercial introduction is planned for November or December 2022. The company's NASP (Neuromorphic Analog Signal Processing) technology had started as a mathematical development of the Chief Scientist and co-founder Dmitry Godovsky. He developed an equation that makes it possible to represent inferencing neural networks using analog elements such as operation amplifiers (Opamps) and resistors.

Based on that concept, Polyn was founded in 2019, and recruited Israeli developers from IBM, Intel, Tower Semiconductors, Cadance etc. The company successfully implemented the new representation by building Analog Neuromorphic Model composed of thousands of digital neurons using classic building blocks: Operational Amplifiers (OpAmp) and Resistors. Polyn's first NASP chip contains 50,000 analog neurons. Timofeev estimates that its power consumption is 100 times better compared to a parallel digital neural network, and 1,000 times faster.

A COMBINATION OF DIGITAL NETWORK AND AN ANALOG PROCESSOR

Since its foundation, Polyn raised $4.5 million, and currently it employs 22 employees. Although registered in UK and holds an office in London, Polyn's headquarters is located in Caesarea, Israel. It is currently in the process of registering 21 different patents to protect its technology. The final product is a hybrid of a fixed analog network for pattern identification, and additional dynamic digital component in charge of interpreting patterns.

This component is also responsible for the addition of new components to the algorithm during updates and even to perform training at some level. Timofeev: "An average of 90% of the neural network is fixed and unchanged. Less the 10% is updated during operation. Our chip is hybrid: we transform 90% of the network to an analog circuit, and the rest remains digital. We can also adjust this ratio according to the specific needs."

THREE CHIPS ROAMAP

The first processor, NeuroSense, will be the first member of NASP family and is planned to reach the market by the end of 2022. Its power consumption is below 100µW, which make it perfect for low-consumption accessories such as smart watches and wearable devices. It will be marketed as a physical component and as an Intellectual Property (IP) offer. "NeuroSense will solve an existing problem within all smart watches: They have to constantly monitor all sensors, something that consume lots of energy."

Polyn's roadmap contains two more components: An Audio Processor, intended to segregate human voice from background voices, and is designed for the hearing aids market, first responders teams, radio communication devices and later also consumer applications. The third chip will focus on shock analysis for the industrial market.

WHAT IS THE IMMUNITY LEVEL OF THE CHIPS?

"We rely on existing, well proven production processes. This is why the production of the first chip is performed in CMOS 55nm technology. We perform 50 inferences per second. This is very low frequency, which makes the component highly immune to electromagnetic interferences. As any other neural network, it is a parallel network, meaning a fault in single neuron does not affect the final result. This is not a circuit that accumulates faults."

PORTFOLIO COMPANY NEWS
RAAAM MEMORY TECHNOLOGIES

CEO Interview: Dr. Robert Giterman

April 29, 2022 by Daniel Nenni - SemiWiki.com

FIRST, PLEASE TELL ME ABOUT RAAAM?

RAAAM Memory Technologies Ltd. is an innovative embedded memory solutions provider, that delivers the most cost-effective on-chip memory technology in the semiconductor industry. RAAAM's silicon-proven Gain-Cell RAM (GCRAM) technology combines the density advantages of embedded DRAM with SRAM performance, without any modifications to the standard CMOS process available from multiple foundries.

RAAAM's patented GCRAM technology can be used by semiconductor companies as a drop-in replacement for SRAM in their SoCs, allowing to significantly reduce fabrication costs through a significant die size reduction. Alternatively, increasing the on-chip memory capacity in the same die size enables a dramatic reduction in the off-chip data movement to resolve the memory bottleneck. This increase in on-chip memory capacity will enable additional features that can enable industry growth for applications in the areas of AR/VR, Machine Learning (ML), Internet-of-Things (IoT), and Automotive.

WHAT PROBLEM ARE YOU SOLVING?

Important industry growth drivers, such as ML, IoT, Automotive and AR/VR, operate on ever-growing amounts of data that is typically stored off-chip in an external DRAM. Unfortunately, off-chip memory accesses are up-to 1000x more costly in latency and power compared to on-chip data movement. This limits the bandwidth and power efficiency of modern systems. In order to reduce these off-chip data movements, almost all SoCs incorporate large amounts of on-chip embedded memory caches that are typically implemented with SRAM and often constitute over 50% of the silicon area. This memory bottleneck is further aggravated since SRAM scaling has been increasingly difficult in recent nodes, shrinking only at a rate of 20%-25% compared to almost 50% scaling for logic.

CAN YOU TELL US MORE ABOUT GCRAM TECHNOLOGY?

GCRAM technology relies on a high-density bitcell that requires only 2-3 transistors (depending on priorities on area or performance). This structure offers up-to 2X area

reduction over high-density 6T SRAM designs. The bitcell is composed of decoupled write and read ports, providing native two ported operation, with a parasitic storage node capacitor keeping the data. Unlike conventional 1T-1C eDRAM, GCRAM does not rely on delicate charge sharing to read the data. Instead, our GCRAM provides an active read transistor that provides an amplified bit-line current, offering low-latency non-destructive readout without the need for large storage capacitors. As a result, GCRAM does not require any changes or additional costs to the standard CMOS fabrication process and scales with technology when properly designed.

While the concept of 2T/3T memory cells has been tried in the past, reduction of the parasitic storage capacitor and concerns about increasing leakage currents has so far discouraged its application beyond 65nm. RAAAM's patented innovations comprise clever circuit design at both memory bitcell and periphery levels, resulting in significantly reduced bitcell leakage and enhanced data retention times, as well as specialized refresh algorithms optimized for various applications, ensuring very high memory availability even under the most extreme operating conditions. In fact, we had demonstrated the successful scaling of GCRAM technology across process nodes of various foundries (e.g., TSMC, ST, Samsung, UMC), including recent silicon demonstrators in 28nm (Bulk and FD-SOI) and 16nm FinFET technologies implementing up-to 1Mbit of GCRAM memory macros.

SILICON STARTUP SOLUTIONS

CAN YOU SHARE DETAILS ABOUT YOUR TEAM AT RAAAM AND WHAT HAS BEEN DONE TO VALIDATE THE GCRAM TECHNOLOGY?

RAAAM founders, including Robert Giterman, Andreas Burg, Alexander Fish, Adam Teman and Danny Biran, bring over 100+ combined years of semiconductor experience. In fact, RAAAM is built on a decade of world-leading research in the area of embedded memories, and GCRAM in particular. Our work on GCRAM technology has been demonstrated on 10 silicon prototypes of leading semiconductor foundries in a wide range of process nodes ranging from 16nm to 180nm, including bulk CMOS, FD-SOI and FinFET processes. Our work on GCRAM is documented by more than 30 peer-reviewed scientific publications in books, journals, and conference proceedings, and is protected by 10 patents.

WHO IS GOING TO USE RAAAM'S TECHNOLOGY AND WHAT WILL THEY GAIN?

RAAAM's GCRAM technology enables a significant chip fabrication cost reduction or highly improved performance, resolving the memory bottleneck for semiconductor companies in various application fields. Since GCRAM is directly compatible with any standard CMOS process and uses an SRAM-like interface, it can easily be integrated into existing SoC designs.

As an example for potential system benefits, we can look at the Machine Learning accelerators domain using a 7nm AI processor integrating 900MB of SRAM on a single die. In this case, the SRAM area constitutes over 50% of the overall die size. Replacing SRAM with RAAAM's GCRAM technology can provide a reduction of up-to 25% of the overall die size, resulting in up-to $35 savings per die.

RAAM MEMORY 7NM CHIP

Alternatively, for memory-bandwidth limited systems, increasing the on-chip memory capacity can bring substantial performance and power improvements. In fact, the required DRAM bandwidth is often inversely proportional to the on-chip memory capacity. With off-chip memory accesses being up-to 1000x more costly in power and latency compared to on-chip data movement, replacing SRAM with 2X more GCRAM capacity at the same area footprint significantly reduces the off-chip bandwidth requirements and enables RAAAM's customers to gain a competitive advantage in the power consumption of their chip.

WHAT IS RAAAM'S ENGAGEMENT MODEL?

RAAAM follows an IP vendor licensing model. Semiconductor companies can license RAAAM's GCRAM technology for a fee and production unit royalties RAAAM implements the front-end memory controller and GCRAM-based hard memory macros according to the customer specifications and delivers a soft RTL wrapper (using a standard SRAM interface), which instantiates the GCRAM hard macros (GDS) and the soft refresh control (RTL). Additionally, the customer receives a characterization report of the hard memory macro and a behavioral model for system-level verification. At present,

RAAAM is working on the implementation and qualification of a GCRAM-based memory compiler, which will enable RAAAM's customers to automatically generate the complete front and back-end views of GCRAM IP and corresponding characterization reports according to customer specifications.

CAN YOU TELL US ABOUT YOUR RECENT ACHIEVEMENTS?

RAAAM has made very exciting progress recently. First, we have been evaluating the benefits of our technology for leading semiconductor companies, which has confirmed our projected substantial improvements from a performance and cost perspective over existing solutions based on SRAM. In fact, we have recently engaged with a very large semiconductor company on a long-term, co-development project and we continue running customer evaluations for various application fields and process nodes. We see growing interest in our technology in a variety of applications, both in very advanced process (7nm and beyond) nodes and in less advanced ones (16nm and higher). Finally, we are extremely pleased to have joined the Silicon Catalyst Incubator, allowing us to gain access to their comprehensive ecosystem of In-Kind Partners, Advisors, and Corporate VC and institutional investor network.

WHAT IS ON THE HORIZON FOR RAAAM?

Our product development roadmap includes full memory qualification in selected nodes of leading semiconductor foundries, based on customer demand. In addition, we have on-going discussions with numerous foundries for further technology migration to their next generation process nodes. Furthermore, we are looking to expand our embedded memory platform and introduce design flow automation based on our memory compiler development efforts. To this end, we are in the process of raising Seed funding to fully qualify our GCRAM technology and to accelerate our company's overall business growth.

A preliminary GCRAM product brief is available upon request, please send an email to info@raaam-tech.com.

Additional information can be found at:
https://raaam-tech.com/technology
https://www.linkedin.com/company/raaam

module work on top of existing standard EDA-based design flow. The output is a GDSII file ready for tape out immediately. Together with that we have developed our design as a BEOL, so the resistor layer is mask programmable and could be replaced independently to optimize cost and time to market. The EDA tool, we call it T-Compiler, is important for time to market today and for our business model in the future. Right now, we are selling chipsets and IP Blocks. By the way, we also see that the market of chiplet solutions could be covered, since SiPs (systems in package) are becoming increasingly common these days.

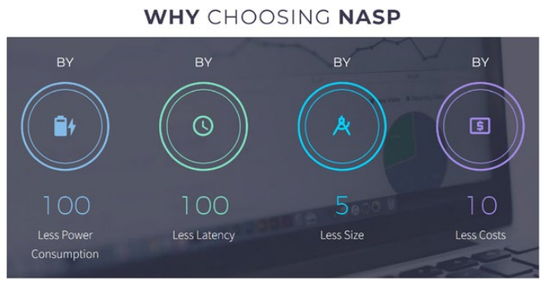
But once the technology is proven and more customers see the advantage of NASP for medium and higher volume products, then our T-Compiler tool will be a part of our business model, enabling generation of application-specific Neuromorphic Analog chips for specific tasks.

Q: GREAT CLARIFICATION, THANKS. LET'S NOW TALK IN GENERAL ABOUT WHEN YOU THINK IT MAKES SENSE TO CONVERT A NEURAL NETWORK INTO SILICON. WHAT APPLICATIONS ARE YOU COVERING BY THE NASP SOLUTIONS?

AT: We focus on any type of one-dimensional signal preprocessing, such as voice, health care sensors, accelerometer, or vibration sensors. And some of our solutions you can evaluate already with simulation that enables evaluation of the chip before its synthesis, to reduce the chance of unexpected behavior. Anyone who is looking for always-on smart sensor data pre-processing is more than welcome to contact us and get access to our D-MVP simulation model. For example, voice extraction and voice detection for hearing assistance demos are functions and running already. So, customers can evaluate and start the design in advance to be ready when the first chip will come from the factory by Q2 of 2023. Customers can also influence the functionality if they are in time to catch the last changes, we are doing these days.

Q: AND WHAT IS YOUR PRODUCT STRATEGY?

AT: Three directions are in our scope of activities for 2023, wearables, hearables, and vibration monitoring for predictive machine maintenance. The first product is planned for mid-2023 and it is our voice extraction solution we announced a week ago. The name of the product line is NeuroVoice and it is intelligent voice extraction and processing for the next generation of smartphones, earbuds, hearing aids, microphones, smart speakers, and intercoms. POLYN's NeuroVoice NASP chip solves the problem of communication in a noisy environment. This differs from noise cancellation and can answer such challenges as irregular noises like animal sounds, babies crying, and sirens. It also solves the problem if the sound comes over the network already mixed with noise. Together with voice extraction, NeuroVoice offers



a combination of voice management features such as voice activity detection, keyword spotting, and others. In addition, the product can be customized for special requirements.

Q: WAS IT EASY TO RAISE MONEY? I KNOW THAT THE SITUATION CHANGES EVERY TIME.

AT: Raising money is never easy (smiling). Of course, we worked hard to communicate with investors. We have a few VCs joining us and several more currently in the due diligence process. That is where we anticipate value in joining the Silicon Catalyst incubator, with the increased exposure we will gain through the incubator's huge portfolio of partners.

Q: WHAT DO YOU THINK ABOUT NEUROMORPHIC CHIPS TODAY? THOSE LIKE INTEL LOIHI, BRAINCHIP AND OTHERS AROUND?

AT: We can discuss other solutions and compare performances, but in general, I can say that in our opinion they are targeted to a more centric position on the edge, with power consumption of a hundred milliwatts to a few watts, but POLYN is focused on the micro-watt level of the thin edge.

Q: AND THE FINAL QUESTION. AS A VISIONARY, HOW DO YOU SEE THE NEURAL-NETWORK- ON-CHIP MARKET AND WAYS OF ITS DEVELOPMENT? WOULD IT BE DIGITAL, IN-MEMORY, OR SIMILAR TO NASP?

AT: For some time, I think, things will run in parallel, and each technology will try to find niches, but finally, in my opinion, the future lies in self-organizing structures, like NASP, but with different physical principles of neurons.

Q: ON THAT NOTE, THANK YOU VERY MUCH, ALEKSANDR.

AT: Thanks a lot for the opportunity, and let's meet in mid-2023 when the first NeuroVoice chip will roll off the line.

PORTFOLIO COMPANY NEWS
LEMURIAN LABS

Lemurian Labs

CEO Interview: Jay Dawani

August 19, 2022 by Daniel Nenni - SemiWiki.com

Jay Dawani is the co-founder & CEO at Lemurian Labs, a startup developing a novel processor to enable autonomous robots to fully leverage the capabilities of modern day AI within their current energy, space, and latency constraints.

Prior to founding Lemurian, Jay had founded two other companies in the AI space. He is also the author of the top rated "mathematics for deep learning" book.

Jay has also served as the CTO of BlocPlay, a public company building a blockchain-based gaming platform, and served as Director of AI at GEC, where he led the development of several client projects covering areas from retail, algorithmic trading, protein folding, robots for space exploration, recommendation systems, and more. In his spare time, he has also been an advisor at NASA FDL.

CAN YOU GIVE US THE BACKSTORY ON LEMURIAN?

We started Lemurian because of the observation that the robotics field is moving towards the adoption of software-defined robots over the large stationary fixed function robots which have been the norm in the last few decades. The main advantage here is the ability to give robots new capabilities over time through training with more simulated data and over the air updates. Three of the biggest drivers for this shift are deep learning and reinforcement learning; more powerful compute; and synthetic data. Most robotics companies are unable to fully leverage the advancements in deep learning and reinforcement learning because of a lack of sufficient compute performance within the power consumption and latency they require. Our roadmap is aligned to these customer needs, and we are focused on building the processor that would address these concerns. In some ways, we are building the processor we would need if we were to launch a robotics company.

THERE HAVE BEEN OVER 100 COMPANIES CREATED IN THE LAST 10 OR SO YEARS THAT ARE FOCUSING ON AI HARDWARE, WHAT MAKES LEMURIAN DIFFERENT?

We are developing a processor that enables AI in robots with far less power and lower latency by leveraging custom arithmetic to do matrix multiplication differently so that it is reliable, efficient, and deterministic. Our approach is well suited to address the needs of the growing autonomous robotics industry which can include anything from a home vacuum cleaner to a materials handling robot in a warehouse or a vehicle outdoors performing last mile delivery. What many of these applications have in common is the need to respond rapidly to changes in its local environment using very low power, and cannot wait for a signal from a data center in the cloud. These applications need to be programmed for their particular context, with high precision and deterministic actions. Determinism in our case means generating the same answer every time given the same inputs, which is essential for safety. General purpose AI processors, as others are building them, do not address these essential requirements.

ARE YOU SAYING THAT THE ROBOTICS INDUSTRY NEEDS A DEDICATED PROCESSOR THAT IS DIFFERENT FROM WHAT MOST AI HARDWARE COMPANIES ARE BUILDING?

Absolutely! Most companies focusing on edge AI inference are over-optimized for computer vision, but the challenge with robotics is that it is more than computer vision where conventionally the objective is for example to detect whether something is present in an image or to classify it. A robot on the other hand is something that interacts with the real world. It has to perceive, decide, plan, and act based on often incomplete and often uncertain information.

For example, a bin picking and sorting robot needs to be able to perceive the difference between objects, and interact with them appropriately with high speed and accuracy. With the availability of a domain-specific compute platform, robots will be able to process more data from sensors in less time which will allow many mobile robots to complete longer missions or tasks, and react to changes in the environment more quickly too. In some applications, it is hard to collect enough good data to train a robot so companies are using behavior cloning which is where a robot learns by observing demonstrations from a human in a supervised setting.

These autonomous robotic applications require an entirely new approach such as the one we are taking with our processor, which has been designed from first principles. Our solution is software-defined, high precision, deterministic, and energy efficient. That is why we are generating so much interest in this market segment from some of the leading companies. Fundamentally, we are doing for deep reinforcement learning inference at the edge what NVidia did for deep learning training in the data center.

VERY COOL. SO WHAT IS UNIQUE ABOUT THE TECHNOLOGY THAT YOU ARE BUILDING?

Fundamentally, we are building a software managed, distributed dataflow machine that leverages custom arithmetic, which overall reduces power consumption and increases silicon efficiency. The demands of AI are so severe now it is breaking the old way of doing things, and that is creating a renaissance in computer architectures reviving ideas like dataflow and non-Von Neumann. A lot of these ideas are commonplace in digital signal processing and high performance data acquisition because these systems are constrained by silicon area or power.

For our target workloads, we were able to develop an arithmetic that is several orders of magnitude more efficient for matrix multiplications. It is ideally suited to modern day AI which depends heavily on linear algebra algorithms, and allows us to make better use of the transistors available. Other linear algebra-dominated application verticals, such as computer-aided engineering or computer graphics require floating-point. But floating-point arithmetic as we know is notoriously energy inefficient and expensive.

WHAT IS THE BENEFIT OF THIS APPROACH OVER THOSE BEING TAKEN BY OTHER COMPANIES?

The arithmetic we designed has roughly the same precision as a 16-bit float but consumes a fraction of the area. In a nutshell we're able to get the efficiency of analog while retaining all the nice properties of digital. And once you change the arithmetic as we have, you can back off the memory wall and increase your performance and efficiency levels quite significantly.

Single precision floats have been very effective for training deep neural networks as we have seen, but for inference most AI hardware companies are building chips for networks that have been quantized to 8-bit integer weights and activations. Unfortunately, many neural network architectures are not quantizable to anything below 16-bit floats. So if we are to squeeze out more performance from the same amount of silicon as everyone else, we need new arithmetic.

Taking some of the newer neural network topologies as an example, the weights and activations in different layers have different levels of sensitivity to quantization. As a result most chips are forced to accommodate multi-precision quantization and have multiple arithmetic types in their hardware which in turn reduces overall silicon efficiency. We took this into account when designing our custom arithmetic. It has high precision, is adaptive and addresses the needs of deep learning to enable training, inference, and continual learning at the edge.

WHY DO YOU THINK OTHER COMPANIES HAVEN'T INNOVATED IN ARITHMETIC?

High-performance systems always specialize their arithmetic and computational pipeline organization. However, general-purpose processors need to pick a common type and stick with it, and ever since IEEE standardized floating-point arithmetic to improve application interoperability among processor vendors in 1985, these common types have been floating-point and integer arithmetic. They work for the general case, but these types are suboptimal for deep learning.

Over the decades companies developing GPUs have had many different types and arithmetic optimizations in the lighting equations, geometry stages, and rasterization stages, all optimizing for area because of the need to multiply these units millions of times. The nature of the number system is the true innovation. The awareness that a particular computation has a particular opportunity to sample more efficiently is a nontrivial exercise. But when the vertex and pixel shaders made the GPU more general purpose, it progressed to the same common arithmetic as the CPUs.

So there has been innovation in arithmetic, but we haven't made the progress in it that we should have. And now we are in an era where we need to innovate not just on microarchitecture and compilers, but arithmetic as well to continue to extract and deliver more performance and efficiency.

YOU JUST CLOSED YOUR SEED ROUND. WHAT CAN WE EXPECT TO SEE FROM LEMURIAN IN THE NEXT 12-18 MONTHS?

We did indeed close an oversubscribed seed round. This was a pleasant surprise given the market situation this spring, but we are starting to hear more use cases and more enthusiasm for our solution from our target customers. And investors are increasingly open to novel approaches which may not have gotten attention years ago before the difficulties of the current approaches were commonly known.

We have built out our core engineering team and are forging ahead to tape out our test chip at the end of the year which will demonstrate our hypothesis that our hardware, software and arithmetic built for robotics can deliver superior processing, at lower energy usage and in a smaller form factor than competitors. We will be taping out our prototype chip at the end of 2023, which we will get into our early customers hands for sampling.

SILICON STARTUP SOLUTIONS

PORTFOLIO COMPANY NEWS
SALIENCE LABS

CEO Interview: Vaysh Kewada

May 20, 2022 by Daniel Nenni - SemiWiki.com

Vaysh Kewada is cofounder and CEO at Salience Labs, a company developing an ultra high-speed multi-chip processor that packages a photonics chip together with standard electronics to enable exascale AI. Salience is funded by Oxford Sciences Enterprise, Cambridge Innovation Capital, Arm-backed Deeptech Labs, former Dialog Semiconductor CEO Jalal Bagherli and former Temasek board member Yew Lin Goh. Prior to launching Salience Labs, Vaysh worked at Oxford Sciences Enterprises, a $745M VC fund focused on deep-tech investments. Prior to that, she was a management consultant at McKinsey & Company. Vaysh holds an undergraduate and Masters degree in Physics from Imperial College London, where her thesis focussed on genetic algorithms.

TELL US ABOUT SALIENCE LABS?

Salience Labs was spun out of Oxford and Münster universities in 2021 to commercialise an ultra-high-speed multi-chip processor that packages a photonics chip together with standard electronics. By using light to execute operations, we can deliver massively parallel processing performance – bringing ultra-high speed compute to a wide array of new and existing AI processes and applications.

The compute requirements of AI double every 3-4 months, as the world needs ever-faster chips to grow AI capability. The current semiconductor industry can't keep pace with this demand. What's required now is not further incremental innovations on transistor technology. If we are to realise the tremendous potential of AI, nothing short of a paradigm shift in the way we compute will do. One that delivers an immediate step change in performance and speed, while also offering a long-term future roadmap of scaling improvements.

Multi-chip processors – ones that package together several platform technologies – is that step-change, allowing us to package electronics together with silicon photonics, and to move compute from electronics to the realm of light. By using light to execute operations, it's possible to achieve massively parallel performance and deliver high throughput, low latency matrix maths – at the root of almost all AI applications. And it's possible to do this with clocking speeds in the 10s of GHz – where currently the limitation of even the most cutting-edge chips is just 2-3 GHz.

WHY WAS SALIENCE LABS FOUNDED?

Salience was founded with the vision of creating an exa-scale processor, by packaging a photonics chip together with standard electronics. The technology is based on decades of research at University of Oxford and Münster University in Germany.

The key inventors and researchers of the technology: Professor Wolfram Pernice, Professor Harish Bhaskaran and Dr. Johannes Feldmann, are co-founders in the company, giving Salience Labs significant depth of knowledge in this field.

WHAT MAKES SALIENCE LABS TECHNOLOGY UNIQUE?

While other photonic chip companies execute operations in the phase of light, we use a proprietary amplitude-based approach to photonics, resulting in modular, dense computing chips clocking at 10's of GHz. It also allows for high levels of parallelization, by using different wavelengths of light to send many calculations through the chip. Salience uses a multi-chip design, with the photonic processing mapping directly on top of the Static Random Access Memory (SRAM). This novel 'on-memory compute' architecture allows for the fast compute in the photonic domain to be fully utilized, delivering an exceedingly dense computing chip without having to scale the photonics chip to large sizes. This architecture can be adapted to the application-specific requirements of different market verticals, making it ideal for realising AI inference use-cases in communications, robotics, vision systems, healthcare and other data workloads.

SILICON STARTUP SOLUTIONS

HOW HAS THE COMPANY EVOLVED SINCE YOU FOUNDED IT?

We originally spun-out of the University of Oxford and the University of Münster in 2021 and have just closed our seed round of $11.5 million from a number of leading VCs including Cambridge Innovation Capital, Oxford Science Enterprises and Arm-backed Deeptech Labs participating, plus some leading names in the semiconductor industry including former CEO of Dialog Semiconductor Jalal Bagherli and Yew Lin Goh. Since closing our seed round, our focus has been on the tape out of our next test chip, developing our software models and packaging solutions. We are also building relationships with customers across a range of market verticals.

YOU ARE PARTICIPATING IN THE SILICON CATALYST INCUBATOR PROGRAMME. WHAT HAS BEEN THE IMPACT ON THE BUSINESS?

We joined the Silicon Catalyst programme in 2021, right after spinning out from Münster and Oxford Universities. The greatest benefit is the access it gives us to advisors – individuals who have made a significant impact on the global semiconductor industry. In fact, we met our chairman Dan Armburst through the programme, who is a Silicon Catalyst Co-founder and Board Director. Through those advisors, we gained highly valuable commercial introductions to foundries, IP providers, and EDA providers at a very early-stage of the company. It has given Salience Labs' a commercial jump start. For example, we've just closed our seed round but we're already working with production level foundries on the fabrication of our next test chip. Silicon Catalyst has been a tremendous accelerator for our business.

WHAT CAN WE HOPE TO SEE FROM SALIENCE LABS IN THE FUTURE?

We're at a very interesting point in time where the industry is recognising the potential of multi-chip processors to solve the tremendous processing bottleneck currently hampering AI growth. Salience Labs' technology has the potential for breakthrough performance and power capability beyond what the established CMOS roadmap offers. We're talking to customers across a range of market verticals who are excited about the performance improvements silicon photonics will offer and the new AI processes and applications this will enable. We welcome any additional approaches from potential customers who are interested in understanding the capabilities of silicon photonics.

PORTFOLIO COMPANY NEWS
OWL AI

CEO Interview: Chuck Gershman

May 13, 2022 by Daniel Nenni - SemiWiki.com

Chuck Gershman is the CEO and co-founder of Owl Autonomous Imaging, Inc. Chuck is a Drexel University College of Engineering inductee into the Alumni Circle of Distinction, the highest honor bestowed upon alumni. He has been honored as a finalist for CMP publications (EE Times) prestigious ACE award as High Technology Executive of the Year and was previously named a Top 40 Healthcare Transformer by Medical Marketing & Media for his work on Clinical AI Decision Support for cancer patients. Chuck holds three US patents for his contributions to Microprocessor Architecture.

Chuck brings over 30 years of technology and semiconductor industry experience in executive management, marketing, engineering, business development, sales, consulting, and executive advising. Including Owl Autonomous Imaging, Mr. Gershman has served as CEO/COO and a Board Director for three companies, he knows what it takes to lead a vision to reality – having led successful exits with acquisitions by Intel and PMC-Sierra.

WHAT IS THE BACKSTORY OF OWL AI?

The foundation of Owl's technology was created under a challenge grant from the US Air Force to track ballistic missiles in flight. Leveraging this technology and the associated patent portfolio, Owl has developed a monocular Thermal Ranging™ camera that provides HD Thermal video with precision ranging that delivers a 150x better spatial resolution than LIDAR (500x that of Radar). A number of our team members come from Kodak where they helped to develop the first commercial digital cameras and first optical scanner. With regards to thermal imaging our team has developed two thermal cameras that are currently deployed in space. The team also recently completed a military uncooled thermal design for one of the most advanced military grade thermal cameras developed to date.

WHAT PROBLEMS/CHALLENGES ARE YOU SOLVING?

We are basically improving sensing and perception of living things such as humans and animals with our 3D dense range map regardless of time of day and regardless of visual impairments such as fog, rain, sleet, snow, exhaust, glare and speed to name some.

WHAT MARKETS DOES OWL ADDRESS TODAY?

Owl addresses automotive safety markets such as ADAS and AV's, industrial off-road markets that require robotic mobility and select military applications. With regards to automotive safety, automatic emergency braking (AEB) has quickly evolved as a must have feature. This capability has now moved from not just automated braking of large objects like cars, busses or trucks but braking for pedestrians and animals. This is known as Pedestrain AEB. Though these systems have been shown to dramatically reduce accidents the current class of systems completely fail when operating at night. Testing completed earlier this year by the Insurance Institute of Highway Safety (IIHS) reported a 32% reduction in pedestrian crashes for systems enabled with PAEB versus those without during the day. However, they also found absolutely no difference in crash rate when operating at night. A complete fail. That is where Owl AI comes in.

WHAT MAKES OWL AI AND OWL AI'S PRODUCTS UNIQUE?

Owl's new monocular ranging sensor system, called the Thermal Ranger, outputs a megapixel (MP) of thermal (night vision) video in parallel with optically fused, 3D range-maps that are similar in appearance to LiDAR and radar range map formats, but delivering orders of magnitude more data points per second. Owl's solution is analogous to recent announcements of 3D single camera computer vision systems operating in the visual domain; however, Owl's Thermal Ranger is unique as it delivers rich detail and 3D response day or night, including operation in extreme visually impaired environments known as DVE.

The Thermal Ranger is composed of a first of its kind Megapixel Digital Focal Plane Array (MP-DFPA) semiconductor chip producing nearly four times the resolution of today's analog-based VGA thermal cameras. The Thermal Ranger also includes a multi-aperture optical component (MLA), and a suite of Convolutional Neural Network (CNN) ranging software for true thermal computer vision. The sensor operates in the thermal spectrum (longwave Infrared) allowing it to see the world clearly, in high-resolution, through adverse DVE and any lighting condition for instant classification and 3D location of pedestrians, cyclists, animals, vehicles, and other objects of interest. This is a true no light system, not to be misconstrued with a low light camera (NIR or SWIR).

This low cost, compact, single lens (monocular) system outputs megapixel HD thermal video producing vivid clarity, while simultaneously generating 3D range maps of up to 90 million points per second, which is orders of magnitude more angular and spatial resolution than LiDAR or radar sensors. For PAEB systems, the novel MLA enables simultaneous capture of both wide angle and telephoto fields of view (FOV) through a single main lens providing wide angle curb to curb response (100 degrees) while enhancing 2D long-range response to well beyond 300 meters and delivering high accuracy 3D range response at distances of over 185 meters. Removal of the MLA along with installation of a telephoto lens with a FOV idealized for long haul highway scenes results in the system being idealized for long haul AV trucking applications with object detection response up to 400m well beyond any other sensor available today including LiDAR.

WHAT'S NEXT FOR OWL AI? OR WHAT IS OWL AI'S FUTURE DIRECTION?

Owl currently has paying customers. Owl recently completed a Series A financing round of $15M to help us accelerate our development and we are focused on executing on our technology roadmap and expanding our go-to-market resources. We are starting to engage higher volume opportunity customers as well as identify and plan for future optimizations of our roadmap with key customer input. We believe our solution is cost effective today and we will continue to align our products with a strong value proposition over the long term.

ADDITIONAL THOUGHTS?

We believe that today's ADAS, AV and Robotic Mobility systems will be improved through the sensor diversity achieved by adding this fourth sensor modality. Lastly, our solutions are being designed with automotive quality standards in mind and we intend to meet the needs of the massive opportunity in this market.

PORTFOLIO COMPANY NEWS
TRAMETO

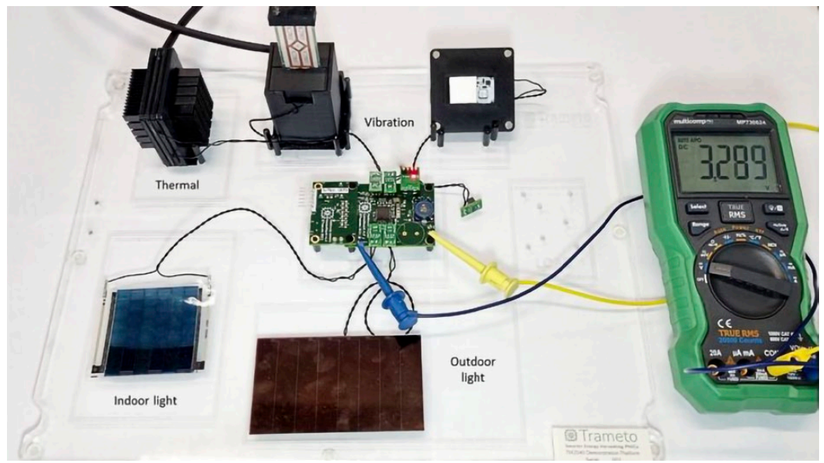
Smarter EH PMICs Trameto

Trameto Demo Unit for EH PMICs

August 4, 2022 by David Manners - ElectronicsWeekly.com

Trameto, a manufacturer of power management semiconductors for energy harvesting (EH PMICs), announces a demonstration platform that enables engineers to quickly evaluate how micro-energy harvesting can reduce or eliminate the use of batteries in IoT devices such as sensors and the wireless modules to which they may be connected.

It is based on Trameto's OptiJoule technology and uses an engineering sample of the TM2040, a four-input, smart EH PMIC from the product family. Up to four harvesters of the same or mixed types can be connected to any of its inputs without additional interface components, providing the simplest, most effective, and most economical way to cut battery dependency in wireless IoT applications. The demonstration platform includes two photovoltaic harvesters, a piezoelectric harvester with a DC motor to generate vibration for it, two thermoelectric generators, and a heater and heatsinks to provide a stimulus for the thermoelectric generators. Each harvester produces microjoules to millijoules of energy and easily connects to the main platform using plugin daughterboards. Uniquely, each of the TM2040's inputs will adapt autonomously to the type of harvester connected to it. The chip then optimizes each harvester's output using patented circuits that also dynamically combine the maximum available energy from all the connected harvesters. The optimized output delivers a controlled charge to an energy-storage component which is then automatically switched via the EH PMIC to power an IoT device with a 1.8V DC, regulated supply at up to 15mA. The demonstration platform comes complete with a Windows application to display harvested power and TM2040 status information from the platform via a simple graphical user interface. Huw Davies, CEO of Trameto, commented: "Energy harvesting can only be economically realized for IoT applications if every available source of energy can be exploited. The TM2040 OptiJoule EH PMIC is the only power management device able to do this economically, replacing up to four traditional PMICs and eliminating the cost and complexity of the interface components that are often needed for some energy harvesters. This demonstration platform provides the easiest way for engineers to explore the opportunities to power their devices using a range of energy harvesting technologies." The TM2040 demonstration platform is available from Trameto now and a user guide can be downloaded https://trameto.com/resources/. A single-input version of the autonomously adaptable PMIC is also available.



SILICON CATALYST ANGELS
INVESTING IN THE INNOVATION

SILICON CATALYST ANGELS

Funding and Fostering the Innovations, Technologies, and Companies that will Improve our Lives

Silicon Catalyst Angels was spawned from Silicon Catalyst, the world's only incubator focused exclusively on accelerating solutions in silicon.

What makes Silicon Catalyst Angels unique is not only our visibility into an exclusive deal flow pipeline, but our membership is composed of seasoned semiconductor veterans who bring with them a wealth of knowledge along with their ability to invest. Driven by passion and desire to "give back", our members understand the hardware space thanks to a lifetime of engagement in the industry. When you couple our members' enthusiasm, knowledge, and broad network of connections with the companies that have been vetted and admitted to Silicon Catalyst, you have a formula that is, to date, non-existent within the investment community.

After launching our group in July 2019, we're pleased to announce that our members have made investment in 13 companies, 11 of which are from the Silicon Catalyst Incubator/Accelerator. The total investment amount by the members is over $2 million.

Interested in joining?
Interested in pitching?

Please contact Laura Swan, VP of Operations
laura@siliconcatalystangels.com
Siliconcatalystangels.com


Amos Ben Meir
Board President


Michael Joehren
Director


Raul Camposano
Director


Laura Swan
VP of Business Operations

Lemurian Labs
Accelerated Computing for Intelligent Robotics
lemurianlabs.com

AyarLabs
Enabling the next phase of Moore's Law through optical connectivity
ayarlabs.com

DOVER MICROSYSTEMS
Stopping Network-Based Attacks with Hardware-based Cybersecurity
www.dovermicrosystems.com

PHINOMICS
Defining the Circulome to Solve Disease
phinomics.com

ESPRE TECHNOLOGIES
Chipsets, Modules, and Sensor Solutions for BoT and IIoT
espretech.com

ERIDAN
The world's most efficient radios for 5G and beyond
eridan.io

MMTRON Powering mmwave Communication
Innovation in mmwave
www.mmtron.com

IMPRINT ENERGY
Printable battery technology for IoT
www.imprintenergy.com

MENTIUM TECHNOLOGIES
Processors for complex video analytics on the Edge
www.mentium.tech

Lelantos
Revolutionizing the world of gas sensing
www.lelantostech.com

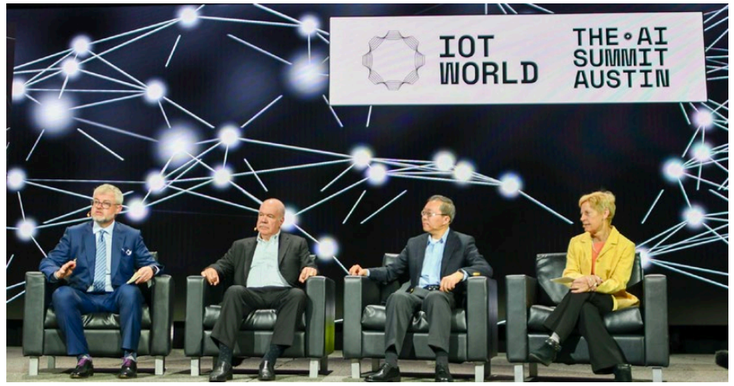
oculi
We see the future
www.oculi.ai

OWL AUTONOMOUS IMAGING
The smartest choice for the road ahead
www.owlai.us

UNIVERSITY NEWS
IoT WORLD AND AI SUMMIT

University of Texas at Austin

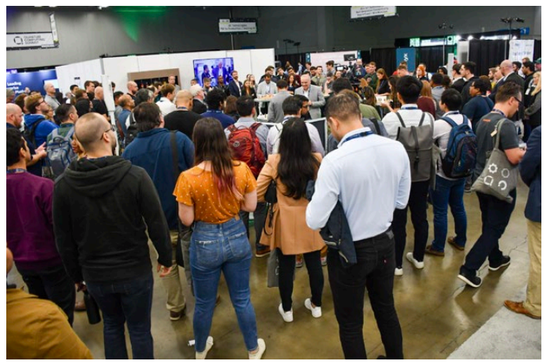
November, 2022 by Pete Rodriquez



University researchers and educators are heading back to their labs. We are reaching out to universities in our ecosystems to reconnect and schedule events as we have in the past. We wanted to give a special thanks to Craig Ensley who has been incredibly helpful with arranging meetings with University professors and stakeholders from both UC San Diego and UC Santa Barbara.

Pete Rodriguez joined Professor David Pan from the University of Texas at Austin during a November visit to the EE department. Pete gave an overview of the CHIPS act, spoke about building an IC company and how Silicon Catalyst and its ecosystem of advisors, in-kind partners and strategic partners can help startups. Dr. Pan shared his support of the idea of making the semiconductor field exciting to students and hopes the CHIPS act funding will help support the training of the future semiconductor workforce.

Pete and David were then joined at the IoT World and AI Summit by Susan Armstrong, SVP for engineering at Qualcomm and Richard Barnett, Chief Marketing Officer, Supplyframe, on a panel entitled “How Far Will the CHIPS Act Stack for the US Tech Economy?”



About Us

Silicon Catalyst is the world's only incubator + accelerator focused on semiconductor solutions, including Photonics, MEMS, sensors, IP and materials. We accelerate startups from idea through prototype, and onto a path to volume production.

We have engaged with more than 800 semiconductor startups worldwide and have admitted 90 exciting companies.

Our companies participate in a 24-month customized incubation program. Each is guided closely by a Silicon Catalyst partner. This includes a semiconductor focused curriculum and over 45 events worldwide each year.

Silicon Catalyst's ecosystem provides everything our startups need to design, fabricate, and market semiconductor solutions:

• **In-Kind Partners** (TSMC, Synopsys, ARM, ST, MathWorks and over 50 more) – provide each startup several millions of dollars' worth of goods and services including EDA tools, IP, PDKs, prototypes, design and test services, packaging and business solutions.

• **Strategic Partners** (including TI, Soitec, Bosch, Cirrus Logic, Arm, ST, Sony, EMD Electronics and NXP) – participate in the selection process and actively look for opportunities to partner with our startups.

• **Investors** – A large group of over 300 VCs, Angels, Angel groups, Corporate VCs, and Family Offices fund each journey. Silicon Catalyst Angels, created from our ecosystem, also funds our companies.

• **Advisors** – A valuable network of over 200 industry experts that we match to the specific needs of each startup.

• **Universities, Industry Organizations, Incubators, and Government Agencies** – We nurture dozens of key relationships for the benefit of our portfolio companies. Our companies have received over $100M in grants.

Silicon Catalyst's mission is to help semiconductor startups succeed. Join us in driving innovation!

Silicon Catalyst Angels was formed to foster the startup companies admitted into the Silicon Catalyst incubator. Comprised of seasoned semiconductor veterans who bring with them a wealth of knowledge along with their ability to invest, they are driven by passion and a desire to 'give back'. Our members understand the hardware space thanks to a lifetime of engagement in the industry. When you couple our members' enthusiasm, knowledge, and broad network of connections with companies that have been vetted and admitted to Silicon Catalyst, you have a formula that is to date, non existent within the investment community.

A VALUABLE RESOURCE FOR THE SEMICONDUCTOR STARTUP COMMUNITY

Si SILICON CATALYST

@SiliconCatalyst

facebook.com/SiliconCatalyst/

linkedin.com/company/silicon-catalyst